Characterization of Interface and Oxide Traps in Ge pMOSFETs based on DCIV Technique

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Abstract — The interface trap density of fresh TiN/TaN gated HfO2/SiO2/Si/epi-Ge pMOSFETs is measured using the DCIV technique. Its temperature dependence is also discussed here. We observe a polarity dependent DCIV peak shift. The bias temperature stress induced interface trapped charge and oxide trapped charge shifts are also systematically investigated in this work.

Index Terms — Ge pMOSFET, interface trap, oxide trap, DCIV.

I. INTRODUCTION

The huge demand to maintain increased transistor density as well as increased saturation current to decrease the switching delay [1] warrants the investigation of alternative channel materials. It has been experimentally validated that germanium offers high hole mobility at higher inversion charge density and, hence, improves the MOSFETs performance [2]-[3]. Recently, Nicolas et al. presented high performance sub-micrometer Ge pMOSFETs with Si monolayers passivated SiO2/HfO2 gate dielectric [3]. However, the high density of pre-existing traps in high-k could lead to a reliability issue. We have recently demonstrated that the high-k gate dielectric is poor when deposited on Ge compared to Si [4]. Moreover, Martens et al. showed the interface trap density is of the order of 1-2x10^13 cm^-2 and resides near the valence band edge [5]-[6]. We also demonstrated that the hot carrier induced damage is a matter of concern due to the low band gap of Ge [7]. Based on all this information, in this work, we look at the post stress interface and oxide charges build up in Ge pMOSFETs. For this purpose the DCIV technique [8] is applied to measure independently the interface and oxide trap charge shifts.

II. DEVICES AND MEASUREMENT

Devices were fabricated using 200 mm Ge-on-Si wafers. A relaxed ~1.6 - 2 µm Ge layer was deposited epitaxially on top of the Si substrate. First, an n-well was formed with a P implants of 1 x 10^13 cm^-2 dose at 570 keV followed by 2.5 x 10^12 cm^-2 at 180 keV. The threshold voltage adjust implant was 4 x 10^12 cm^-2 at 90 keV with P. The Ge surface was passivated with 6 MLs of epi Si grown at 500 °C using SiH4 as a precursor, followed immediately by oxidation in slightly ozonated water to get approximately 0.5 nm SiO2. Immediately after, 4 nm HfO2 was deposited by atomic layer deposition (ALD). The gate metal consisted of TiN/TaN. A P dose of 4 x 10^12 at 60 keV was used for halo to control the short channel performance. A detailed process flow can be found elsewhere [3]-[5]. The device characterizations were done using a Keithley 4200 semiconductor characterization system. In Fig. 1, a schematic diagram of the Ge-on-Si pMOSFET along with the DCIV measurement setup [9] used in this work is shown. The DCIV technique described in [8] is used here with source well and drain well as emitter junctions and the n-well as base contact. This is called top emitter DCIV configuration (TE-DCIV). Here, the base current (Ib) is measured by sweeping the gate voltage (Vg) from inversion to accumulation by applying small forward bias (Ve) to the emitter junction. All the measurements were done on 10 µm x 1 µm MOSFETs at room temperature (RT) unless stated otherwise.

III. RESULTS AND DISCUSSION

Figure 2 shows the normalized TE-DCIV and DE-DCIV (here only drain acts as emitter) curves for fresh TiN/TaN gated HfO2/SiO2/Si/epi-Ge pMOSFETs. Here, ΔIb (= Ib - Ib_{baseline}) is normalized by ΔI_{fwd}. TE-DCIV shows a better behaved bell shaped curve with narrow line width compared to DE-DCIV curve.
with the DE-DCIV mode. For this reason we will use the TE-DCIV configuration throughout our next discussion. The \( \Delta I_{B\text{peak}} \) value is approximately related to the interface trap density \( (N_i) \) by the equation \cite{9}:

\[
\Delta I_{B\text{peak}} = \frac{q N_i W L n \sigma_{\text{th}}}{2} \left[ \exp \left( \frac{q V_e}{n k T} \right) - 1 \right]
\]

(1)

where \( q \) is the electronic charge, \( W \) and \( L \) are the width and length of the transistor, \( n \) is the intrinsic carrier concentration, \( V_{\text{th}} \) is the thermal velocity, and \( \sigma \) is the capture cross-section. \( n \) is a parameter around 1.8-2 introduced by Zhu et al. \cite{9}.

The distinct peak in Fig. 2 indicates that our fresh Ge pMOSFET has a high density of interface traps \( (N_i) \). Now, to calculate the \( N_i \) we determine the parameter \( n \) by studying the temperature dependence of \( \Delta I_{B\text{peak}} \) in the next section.

![Graph of typical DCIV curve of a Ge pMOSFET with emitter forward bias \( V_e \) at 0.2 V. TE-DCIV shows well behaved narrow width DCIV characteristic.](image)

Assuming the relations mentioned below \cite{10}:

\[
\Delta I_{B\text{peak}} \propto T^{-2.5} \left[ \exp \left( \frac{-E_A}{k T} \right) \right]
\]

(2)

and

\[
\Delta I_{B\text{peak}} \propto \left[ \exp \left( \frac{q V_e}{n k T} \right) \right]
\]

(3)

we have plotted the \( \Delta I_{B\text{peak}}/T^{-2.5} \) vs. \( 1/T \) for different \( V_e \) ranging from 0.1 V to 0.25 V in Fig. 3. The slope gives the activation energy \( (E_A) \). From Fig. 4 we can see that the \( \Delta I_{B\text{peak}} \) of Ge pMOSFETs strongly depends on the temperature in the range 298 K to 343 K. Finally, using equation (2) and (3) we have plotted the activation energy \( (E_A) \) with respect to \( V_e \) in Fig. 4. By linear fitting the data in Fig. 4 we obtain the value of \( n \) approximately equal to 2, indicating a pure surface recombination origin. In Fig. 4, Si reference data from \cite{10} has also been included for comparison. An interesting observation is found in Fig. 4 which is the relation between the activation energy and band gap \( (E_g) \). For Ge pMOSFETs, we found the activation energy depends on \( E_g/2 \) whereas for Si in ref \cite{10} it depends on \( E_g \).

Now, from Fig. 1, by using the value of \( n \), and taking equal to \( 5 \times 10^{17} \text{cm}^{-2} \) \cite{5} we found \( N_i \) approximately equal to \( 6.9 \times 10^{13} \text{cm}^{-2} \) for our Ge pMOSFETs. Martens et al. reported the value of \( N_i \) equal to \( 1-2 \times 10^{13} \text{cm}^{-2} \) for similar Ge devices using full conductance measurements \cite{6}, and \( 6 \times 10^{12} \text{cm}^{-2} \) using the charge pumping (CP) technique at 80 K \cite{5}. The factor of 3.5 differences in \( N_i \) between TE-DCIV and full conductance measurements, and one order differences from CP is justified because of the differences in the measurements techniques.
On the other hand, the shift in oxide trap charge ($\Delta N_{ot}$) due to the application of stress is given by [9]:

$$\Delta N_{ot} = \frac{C_{ox} \Delta V_{Gpeak}}{q}$$ (4)

where $C_{ox}$ is oxide capacitance per unit area, $q$ is electron charge, and $\Delta V_{Gpeak}$ DCIV peak voltage shift.

In Fig. 5, $\Delta I_B$ vs. $V_G$ is plotted with $V_e = 0.2$ V for different stress cycles at a stress voltage -2.25 V and 2 V. One can see that along with the DE-DCIV peak increments (due to the increase of the interface trap density) there is a consistent $\Delta V_{Gpeak}$ shift due to $N_{ot}$ build up. It is clear from Fig. 5a, that negative gate voltage stress in Ge pMOSFETs gives rise to hole trapping as the DCIV peak shifts in the negative $V_G$ direction.

On the other hand, for a positive stress electron trapping dominates, as the DCIV peak shifts to the positive $V_G$ direction. We also observed de-trapping of both electrons and holes during our experiments which may occur from shallow trap levels.

It is already known that the threshold voltage instability is strongly process dependent. To know the $N_{it}$ and $N_{ot}$ build up with positive and negative gate stresses in the Ge pMOSFETs, we have calculated independently $\Delta N_{it}$ and $\Delta N_{ot}$, applying equations (1) and (4) and plotted the results as a function of stress time in Fig. 6. Fig. 6 shows the interface trap generation for both positive and negative stress biases. Our analysis shows the initial $N_{it}$ shift due to accumulation stress bias is high and then it gradually slows down. This may be due to a de-trapping effect. It is also observed that $N_{ot}$ increases continuously when stress time increases during the negative voltage stress. However, $N_{it}$ saturation is possibly due to de-trapping when the stress voltage is positive.

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**Fig. 5.** $\Delta I_B$ - $V_G$ plot of Ge pMOSFETs using TE-DCIV technique. a) Shows DCIV peak shift to the left direction when the applied stress bias is negative. This indicates hole trapping in the oxide. b) Shows DCIV peak shift to the right direction which implies electron trapping in the gate oxide.

**Fig. 6.** Time evolution of $N_{it}$ and $N_{ot}$ of Ge pMOSFETs measured from TE-DCIV peak current at emitter forward bias 0.2 V. a) For negative stress bias at -2.25 V. b) For positive stress bias at 2 V.
The degradation behavior of Ge pMOSFETs due to Negative Bias Temperature stress is also studied using the TE-DCIV technique and shown in Fig. 7. Here, the time evolution of $N_t$ using TE-DCIV and the degradation of $I_{\text{I}_{\text{Dlin}}}$ is compared for two stress biases (-2.3 V and -2.5 V) at a temperature 85 °C. $I_{\text{I}_{\text{Dlin}}}$ was measured using the standard on the fly technique at $V_{\text{GS}} = -0.03$ V and $V_{\text{GS}} = -0.8$ V. Increase in stress bias accelerates the $N_t$ and $I_{\text{I}_{\text{Dlin}}}$ degradation with comparable slope and hence Fig. 7 shows a good correlation between the two techniques. It is seen from Fig. 6a and Fig. 7 that negative gate bias stress applied at 85 °C accelerates the degradation compared with room temperature, which may be due to the increase of the hole energy.

![Fig. 7. Interface trap build up (measured from TE-DCIV $\Delta I_{\text{I}_{\text{peak}}}$ increment) and $I_{\text{I}_{\text{Dlin}}}$ degradation (measured at $V_{\text{DS}} = -0.03$ V and $V_{\text{GS}} = -0.8$ V) when a Ge pMOSFET is stressed at $V_{\text{Gstress}} = -2.3$ V and -2.5 V @ 85°C. A good correlation between the two techniques is observed.](image)

VII. CONCLUSION

The DCIV technique has been applied on Ge pMOSFETs. The peak DCIV of Ge pMOSFETs strongly depends on temperature in the range 298 K - 343 K. The activation energy of Ge pMOSFETs base current peak depends on $E_G/2$ unlike for Si. The interface trap density calculated from the DCIV peak is factor 3.5 to one order higher than the value measure from full conductance measurements and CP technique respectively. Polarity dependent oxide trapping due to stress bias is also observed using DCIV. Our measurement suggests that the degradation of interface traps measured by DCIV is well correlated with standard on the fly $I_{\text{I}_{\text{Dlin}}}$ degradation.

REFERENCES