Configurable Low Noise Amplifier for Voltage Noise Measurements

G. Scandurra, G. Cannatà, G. Giusi, C. Ciofi
Dip. Ing. Elettronica, Chimica e Ingegneria Industriale
University of Messina
Messina, Italy
gscandurra@unime.it

***Abstract*—The noise performances of monolithic operational amplifiers are generally insufficient for the realization of low noise amplifiers for applications in the field of low frequency voltage noise measurements. In order to obtain very low levels of equivalent input voltage and current noise, discrete JFETs input stages can be used, with the disadvantage of introducing a large input capacitance that can reduce the usable bandwidth in the case of large source impedances. In this work we propose to employ a modular design entirely based on monolithic operational amplifiers that allows, by paralleling and/or combining in a proper way a number of identical basic amplifier blocks, to reach different compromises in terms of background noise and input capacitance while enabling, at the same time, differential measurement configurations and/or cross correlation background noise reduction approaches.**

Keywords—low noise voltage amplifier, low frequency noise measurements, cross correlation.

I. INTRODUCTION

The Background Noise (BN) of a voltage noise measurements system is set by the equivalent input noise sources of the high gain voltage amplifier used to rise the signal generated by a Device Under Test (DUT) up to a level compatible with the input range of a spectrum analyzer. Especially in the case of low frequency noise measurements (frequency f close or below 1 Hz), the BN is dominated by the flicker noise introduced by the active devices in the first stage of the voltage amplifier. It is for this reason that in many designs the first stage is based on discrete devices. While BJTs may allow to obtain the lowest level of voltage noise at very low frequencies (3 nV/√Hz and 1.5 nV/√Hz at f= 100 mHz and 1 Hz, respectively [1]), the much lower levels of bias current and current noise make JFET input stages preferable when the DUT impedance is above a few hundreds ohms and/or DC coupling to the DUT is not possible[2]. A few designs of JFET based low noise voltage amplifiers have been proposed both for single ended [3] and differential noise measurements [4] with noise performance that can be as low as 1.4 nV/√Hz at f=1 Hz and 14 nV/√Hz at f= 100 mHz. Notwithstanding these excellent noise performances, there are a few aspects in these approaches that may became a limitation in a number of applications. For instance, the equivalent input capacitance is relatively high (400 pF in the amplifier in [3]). This fact limits the usable bandwidth in the case of large impedance DUTs in situations in which a lower input capacitance, even at the cost of a higher BN level would be desirable. Moreover, large area JFETs such as IF3601 or IF3602 are not easily found in general electron devices distribution catalogs and are quite expensive. Finally, even if an effort has been done in order to reduce the complexity of the design to a minimum, the solutions proposed in [3] and [4] still require some skill in terms of circuit prototyping if compared to designs involving only operational amplifiers as active devices. Sometimes, a few discrete active devices can be combined in parallel in order to reduce the Equivalent Input Voltage Noise (EIVN) at the cost of an increase in the Equivalent Input Current Noise (EICN). If the devices we use are characterized by a very low EICN to begin with, the increase in EICN is well compensated by the corresponding reduction in the EIVN[5]. A similar approach could be attempted starting from conventional Operational Amplifier (OA) voltage amplifier stages combined as shown in Fig. 1. With a proper choice of the resistor values R_1, R_2 and R_3, the amplifier in Fig. 1 behaves as a voltage amplifier with the following parameters:

$$A_V = 1 + \frac{R_2}{R_1};\ S_{iEQ} = NS_{iOA};\ S_{vEQ} = \frac{S_{vOA}}{N};\ R_{OUT} = \frac{R_3}{N} \quad (1)$$

where A_V is the voltage gain from the input V_{IN} to the output V_{OUT} (with no load connected), S_{iEQ} and S_{vEQ} are the Power Spectral Densities (PSDs) of the overall EICN and EIVN of the resulting amplifier, respectively, S_{iOA} and S_{vOA} are the PSDs of the EICN and the EIVN of each OA, respectively, N is the number of stages combined together in Fig. 1 and R_{OUT} is the output resistance of the resulting amplifier. The fact that the output resistance is not very low, as it would be at the output of each single OA, and therefore the fact that A_V would change due to loading, can be easily overcome by resorting to an output buffer or a second voltage amplifying stage. The feasibility of such an approach depends on the number of stages N that is required to obtain a low frequency EIVN comparable to that of a discrete JFET input amplifier such as

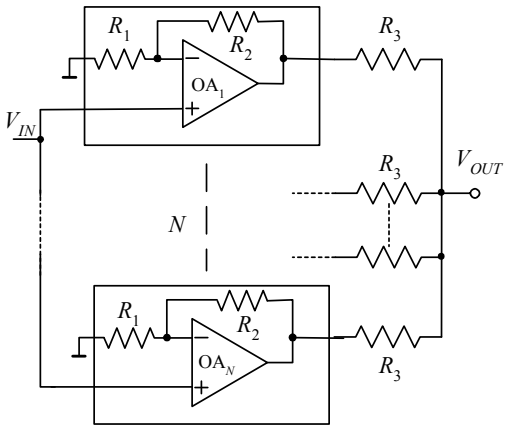

Figure 1. Combination of low EICN operational amplifiers for reducing the overall EIVN.

the one reported in [3]. If we take into consideration the very low EICN TLC070 operational amplifier, for instance, we obtain that for reducing the noise from its 60 nV/√Hz at 1 Hz down to 1.4 nV/√Hz [3], N should be in the order of 1800, which makes this approach, to say the least, unpractical. Note, however, that even with such large N, the current noise would still be in the order of 26 fA/√Hz, that is comparable, if not lower, to that of the popular AD743 FET input OA at frequencies close to 1 Hz. On the other end, with an input common mode capacitance in excess of 20 pF, the equivalent input capacitance with N=1800 would be in the order of 400 nF, that would be completely unacceptable. To the best of our knowledge, until recently, the approach suggested in Fig. 1 was unpractical regardless of the selection of the OA: either the EIVN was too large (N in the order of a thousand) or, for OA with lower EIVN, the EICN was too large, limiting N to a number insufficient to reduce the equivalent EIVN to values close to those obtained in discrete component based low noise preamplifiers. With the introduction of a new generation of very low noise JFET input OA such as the OPA140 series by Texas Instruments, however, the limitations mentioned above are removed and the approach in Fig. 1 becomes feasible. Indeed, the OPA140 is characterized by an EICN similar to that of the TLC070 (0.8 fA/√Hz) with a significantly lower level of EIVN (less than 16 nV/√Hz at 1 Hz and just 50 nV/√Hz at 100 mHz), combined with a low input common mode capacitance of 7 pF. The OPA4140 contains 4 OPA140 amplifiers in a very small TSSOP-14 or SO-14 package. Therefore, by resorting to 16 OPA4140 (N=64) we can reach an EIVN of less than 2 nV/√Hz at 1 Hz and about 8 nV/√Hz at 100 mHz, with an equivalent input capacitance of less than 450 pF obtaining therefore performances comparable to, or even better than (depending on the frequency range), those of one of the best JFET input amplifiers for low frequency noise measurements reported in the literature [3].

In this work we propose a modular design based on the OPA4140 that can be used to obtain different compromises in terms of input capacitance and EIVN with the added interesting feature of enabling fast reconfiguration of the system in order to obtain a number of measurement configurations for performing, besides conventional voltage noise measurements, also cross correlation measurements and/or differential noise measurements.

II. MODULAR AMPLIFIER BUILDING BLOCKS

A single OPA4140 can be used for building an amplifier stage that will be used as a basic Amplifier Block (AB) for the implementation of a number of measurement configurations. Assuming the EICN sources of the amplifiers to be negligible, we can write the power spectrum density of the EIVN of the entire amplifier in Fig. 1 as follows:

$$S_{vEQ} = \frac{1}{N}\left\{ S_{vOA} + 4KT\left[R_1\left(\frac{A_V - 1}{A_V}\right)^2 + \frac{R_2}{A_V^2} + \frac{R_3}{A_V^2}\right]\right\} \qquad (2)$$

where k is the Boltzmann constant, T the absolute temperature and A_V=1+R_2/R_1. With A_V >>1, as it is desired in designing a low noise voltage amplifier, and assuming R_3 in the same order as R_2, (2) becomes:

$$S_{vEQ} \approx \frac{1}{N}\left\{ S_{vOA} + 4KTR_1\left[1 + \frac{1}{A_V}\left(1 + \frac{R_3}{R_2}\right)\right]\right\} \approx \frac{S_{vOA} + 4KTR_1}{N} \qquad (3)$$

With R_1=100 Ω and R_2=10 kΩ, we have A_V=101 and a negligible contribution by R_1 to S_{vEQ}, (1.3 nV/√Hz with respect to a minimum value for S_{vOA} of 6.5 nV/√Hz for f>100 Hz). The network made by the resistances R_3 at the output of the amplifiers allows to obtain the average of the voltages at the output of each single OA, so that the overall voltage gain remains A_V regardless of N. The value of R_3, together with N, sets the value of the output impedance and of the noise added at the output of each amplifier. From these points of view, the lowest possible value of R_3 would be desirable. However, the value of R_3 also sets the value of the DC current I_{ODC} at the output of each amplifier because of the values of the offset voltage at the input of each OA. It can be easily demonstrated that the current I_{ODC} is such that:

$$|I_{ODC}| < \frac{2v_{ioff}A_V}{R_3} \qquad (4)$$

where v_{ioff} is the maximum input offset voltage (220 μV for the OPA4140). With R_3=1 kΩ (R_3<R_2) the maximum value of $|I_{ODC}|$ is less than 100 μA, resulting in a negligible contribution to the EIVN (R_3<<R_2).

The measured EIVN of the basic AB is reported in Fig. 2 (curve with N=4) and is compared with the EIVN that is measured when just one of the OA in the OP4140 package is used for realizing a voltage amplifier (N=1). The EIVN that is obtained with N=16 and that could be obtained with N=64 are also reported in Fig. 2, together with the EIVN of the low noise

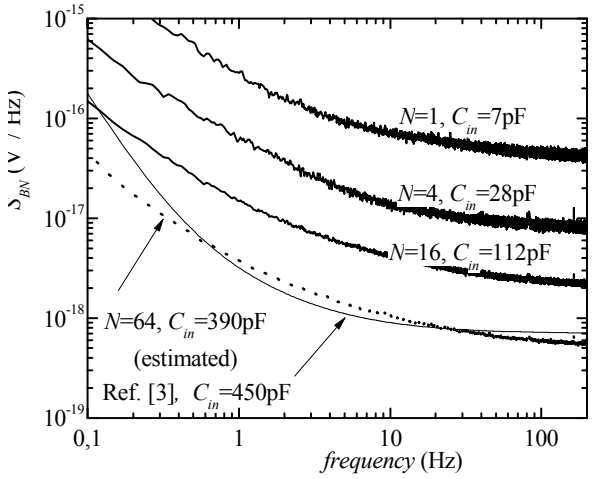

Figure 2. Measured EIVN of the circuit in Fig. 1 for N=1, 4 and 16. The spectrum with N=64 is estimated. The EIVN of the low noise amplifier in Ref. [3] is also reported for comparison. C_{in} is the equivalent input capacitance of the system.

preamplifier in [3] as a reference. As it can be noted, with N=64 we can obtain noise performances comparable to the amplifier reported in [3] with a comparable value of the equivalent input capacitance C_{in}.

Four independent AB blocks can be hosted in a small sized printed circuit board (8×3 cm) with four independent inputs and outputs as illustrated in Fig. 3. This simple arrangement can be used for implementing a number of measurement configurations by adding a few external components as illustrated in Fig. 4. The RC high pass filters in Fig, 4 are needed for rejecting the DC component at the DUT side and the DC component due to the offset at the output side. In all measurements, the high pass filters were obtained with C=22 μF and R=3.3 MΩ. With these values, (high pass corner frequency at 2 mHz), a negligible contribution to the BN for f>100 mHz is obtained[3].

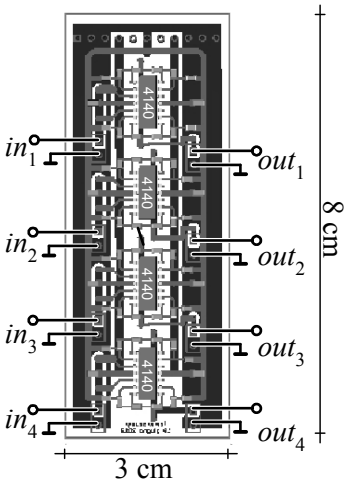

Figure 3. Layout of the printed circuit board hosting four AB. Input and output connections for each AB is also indicated.

It is important to notice that each AB in Fig. 4 can be replaced with an entire board (N=16) obtained by paralleling all the inputs and outputs ports in Fig. 3, thus allowing to reach even lower levels of EIVN if a higher input capacitance can be tolerated.

For testing the board in Fig. 3 in all the configurations reported in Fig. 4, we used a single 1 kΩ resistor as a single ended DUT (Fig. 5a) and the three 1 kΩ resistors combination in Fig. 5b as a DUT requiring a differential input amplifier for measuring the PSD e_{ndif}. At room temperature, the PSDs to be measured are:

$$\begin{aligned} S_{vnse} &= 4kTR = 1.66\times10^{-17}\ \mathrm{V^2/Hz};\\ S_{vndiff} &= \frac{2}{3}\times 4kTR = 1.11\times10^{-17}\ \mathrm{V^2/Hz}; \end{aligned} \tag{3}$$

We explored, in particular, the frequency range from 100 mHz up to a few tens of Hz where the flicker noise introduced by the amplifier dominates.

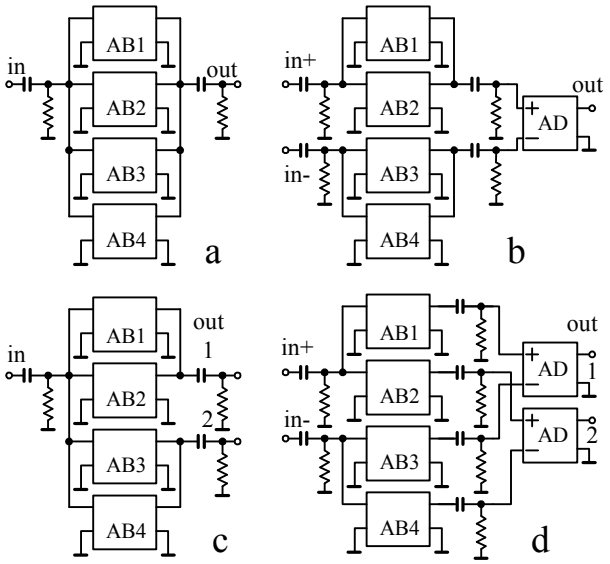

Figure 4. Possible measurement configurations: a) conventional/single ended; b) conventional/differential; c) cross correlation/single ended; d) cross correlation/differential.

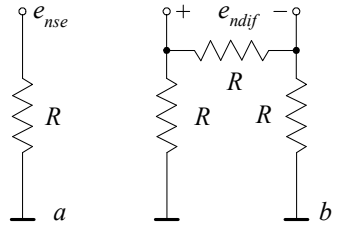

Figure 5. Simulated DUTs for tesing the performances of the amplifier in single ended (a) and differential (b) configurations. R=1 kΩ.

The results of input referred voltage noise measurements performed in configurations a and c (single ended) are reported in Fig. 6. The spectrum obtained when using a 1 kΩ resistor as a DUT and a single AB as an amplifier is also reported in the figure. The beneficial effect of reducing the EIVN (configuration a) with respect to the case in which a single AB is used is apparent. When using configuration c, we can resort to cross correlation between outputs 1 and 2 in order to eliminate the contribution of the uncorrelated noise sources. The averaging time required to reduce the contribution of the uncorrelated noise down to a negligible level with respect to the noise level to be detected, depends on the magnitude of the uncorrelated noise itself. The cross spectrum reported in Fig. 6 required an averaging time of about 1 hour (the resolution bandwidth was 25 mHz). The advantage in paralleling many OA as in Fig. 4c (N=8 for each measurement channel) is apparent when we note that the averaging time required for obtaining the same residual error with the same resolution bandwidth starting form a single OPA140 OA for each channel would have been in the order of 3 days [6]. On the other hand, if we implement the circuit configuration in Fig. 4c with each AB (N=4) replaced by the parallel combination of 4 AB, the measurement time would be reduced to just 250 seconds.

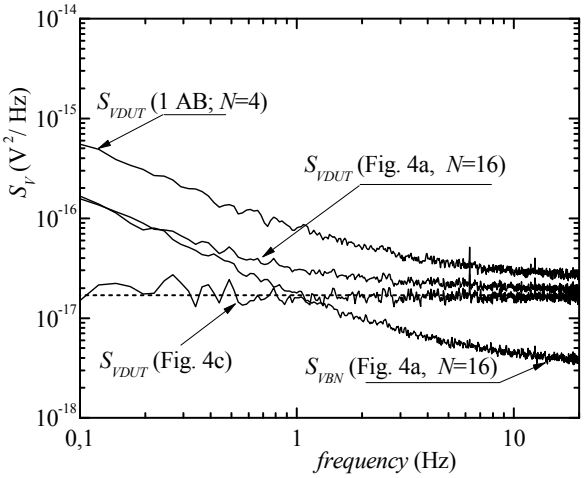

Figure 6. Results of noise measurements on a single ended DUT (1 kΩ resistor). S_{VDUD} does not coincide with S_{vnse} (dotted line) in (3) because of the background noise of the amplifiers. The bacgkround noise S_{VBN} in the configuration in Fig. 4a is also reported in the figure.

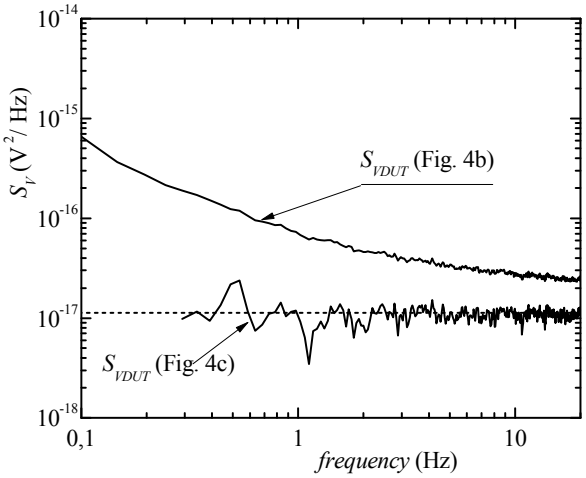

Figure 7. Results of noise measurements on a differential DUT (Fig. 5b). S_{VDUD} does not coincide with S_{vndiff} (dotted line) in (3) because of the background noise of the amplifiers.

The result of input referred voltage noise measurements performed in configurations b and d (differential) are reported in Fig. 7. The noise to be measured is in the same order of the noise to be measured in the single ended configuration. In can be noted that the noise measured in configuration b is dominated by the noise introduced by the amplifier. The measured spectrum in this situation is comparable to the noise spectrum reported in Fig. 6 and relative to single ended noise measurement when using a single AB. This is consistent with the fact that the expected BN in configuration b is twice the noise of each measurement channel made of the parallel of two AB. If we resort to cross correlation (Fig. 4d) we can indeed obtain a spectrum that is quite close to the expected one (dashed line in Fig. 7). It must be noted that, with respect to the single ended cross correlation configuration in Fig. 4c, the uncorrelated superimposed to the noise to be measured at each output is now 4 times larger (twice the noise of a single AB) and therefore the measurement time for obtaining sensible results becomes much larger. The cross spectrum reported in Fig. 7 has been obtained with an averaging time of about 3 hours and with a resolution bandwidth of 25 mHz. Note that, as before, by replacing each single AB in Fig. 4d with the parallel combination of 4 AB, a quite accurate estimate of the DUT noise could be obtained in a matter of a few minutes.

III. CONCLUSIONS

In this paper we have discussed the possibility of designing an ultra low noise voltage preamplifier for low frequency noise measurements without resorting to discrete JFETs. In the design we have proposed we have taken advantage of the excellent performances of the OPA4140 operational amplifier in order to design a modular system that, by combining a number of basic amplifier blocks, can be used for the implementation of the most common low frequency noise measurement configurations. Actual measurements performed on a reduced sized prototype (4 AB) demonstrate the sensibility of the approach we propose and allow to conclude that by employing just 16 AB, that can be contained in four small PCB boards (3×8 cm), noise performances similar to those of the best low noise amplifier based on discrete devices input stages can be obtained.

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