Review

Impact strain engineering on gate stack quality and reliability

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A B S T R A C T

Strain engineering based on either a global approach using high-mobility substrates or the implementation of so-called processing-induced stressors has become common practice for 90 nm and below CMOS technologies. Although the main goal is to improve the performance by increasing the drive current, other electrical parameters such as the threshold voltage, the multiplication current, the low frequency noise and the gate oxide quality in general may be influenced. This paper reviews the impact of different global and local strain engineering techniques on the gate stack quality and its reliability, including hot carrier performance, negative bias temperature instabilities, time dependent dielectric breakdown and radiation hardness. Recent insights will be discussed and the influence of different strain engineering approaches illustrated.

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1. Introduction

Strain engineering has definitively gained an important place in sub-100 nm CMOS technology nodes, as it provides a convenient
means to boost up the device performance [1]. Several techniques are in use, which can be divided in global wafer-level and local, device-level techniques, whereby the latter provide a better scalability. The global approach generally results in biaxial stress in the transport plane, while local stressors generate uniaxial stress in the channel direction. The latter is usually more effective in translating strain into performance enhancement for short channel transistors.

The global approach can be achieved by using epitaxial SiGe layers on a silicon substrate (pMOSFETs) or a strained Si layer (sSi) on a strain-relaxed SiGe buffer (SRB) or even directly on a buried oxide. Whether or not an SRB layer is used underneath will have an impact on the density of both misfit (MD) and threading dislocations (TDs). The standard approach uses a graded Ge concentration resulting in a buffer layer with a thickness in the 1–3 \( \mu \text{m} \) range [2]. Ge concentrations have to be limited to 20–30\% in order to control possible stress relaxation and to restrict self-heating effects due to the lower thermal conductivity of the SiGe epi-layer. A restriction of the self-heating can be achieved by using an alternative technique based on thin SRB layers with 20\% Ge and a thickness around 200–300 nm on top of which 8–12 nm strained Si is grown [3]. Compared to the thick film approach this leads to a 50\% reduction in thermal resistance, without compromising the device performance [4]. Recently, the feasibility of using strained Si either directly on Si (sSO) or on SiGe on Si in order to improve the self-heating behavior has been reported [5]. In recent years, interest has also been triggered to fabricate high-performance devices using Ge-based substrates such as e.g. bulk Ge, Ge-on-Insulator (GeOI) or sGeOI [6]. Generally, the use of so-called high-mobility substrates enables to achieve much higher stress levels compared to the implementation of processing-induced stressors, which are addressed in the next paragraph.

The potential of local compressive strain, based on the embedded or recessed SiGe source/drain (S/D) method in p-channel transistors has been demonstrated at the 22 nm node and beyond [7]. For n-channel devices, requiring tensile strain for electron mobility and drive current enhancement, embedded source/drain regions can be formed by using epitaxial SiC or Si\(_{1-y}C_y\) stressors with y between 1\% and 2\% [8,9]. Compared to SiGe S/Ds the problem of possible Ge outdiffusion is avoided, but replaced by a hazard of C precipitation and creation of C-related interface states. The recessed layer approach has also a positive impact on lowering the series resistance. In other cases, SiN-based contact etch stop layers (CESL), silicide or STI stressors are employed to create uni- or biaxial strain in the channel. Depending on the hydrogen content of the CESL either compressive (c-CESL) or tensile (t-CESL) caps are obtained, so that with a dual cap-layer approach performance optimization is achieved for both p- and n-channel devices. An interesting feature to mention is that there also exists a stress memorization effect, whereby one can continue to rely on the stress after its source has been removed such as, e.g., in the case of disposable trench isolation (STI) regions. Finally, a combination of global and local or different local techniques generally leads to additive stress effects. The drawback may be the more complex process optimization required.

Recent results [11–13] indicate that strain engineering can lead to worsened negative bias temperature instability (NBTI) of pMOSFETs. In the case of p-channel devices with SiGe buffer layers an enhanced hot carrier degradation compared to standard bulk devices is reported [13] due to a higher impact ionization current. The latter may be related to the enhanced mobility, lowering the drain voltage at the pinch-off region and thus resulting in an increase of the ratio of the substrate current over the drain current [14]. Also 1/f noise, which is sensitive to the gate oxide and interface quality, has been found to be degraded in strained devices [15,16].

The present paper reviews recent insights concerning the reliability and gate oxide quality of strained CMOS technologies. Some aspects were discussed before [17] but have been reviewed and

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**Fig. 1.** Schematic representation of the different strain-engineering approaches: (a) global strain, using a tensile strained-Si (sSi) \((x > 0.5)\) or compressively strained-Ge (sGe) layer \((x > 0.5)\) fabricated on a silicon or silicon-on-insulator substrate. The Si or Ge layer may be directly on the buried oxide (BOX); (b) local tensile or compressive stress induced by a SiN cap layer in the Si or SiGe channel; (c) local tensile or compressive strain induced by embedded Si\(_{1-y}C_y\) or Si\(_{1-x}Ge_x\) source/drain regions.

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further elaborated in depth. The first section deals with the impact of strain on certain transistor parameters, like the threshold voltage, and the gate and the multiplication current which are of direct interest for the reliability. The next part handles the impact of strain engineering on the gate oxide quality, assessed by techniques like low-frequency noise, charge-pumping, etc. The section dealing with reliability will focus on hot-carrier and uniform degradation, with special emphasis on negative bias temperature instability (NBTI). Recently, also interest in the radiation hardness has resulted in a few dedicated studies. In the conclusions, key aspects of the impact of strain engineering on gate stack quality and reliability studies are briefly summarized.

2. Impact of strain engineering on material and device characteristics

2.1. Impact on the threshold voltage

The impact of strain on the carrier mobility and band gap structure is well-documented in the literature [1,18]. However, also other device parameters, like the threshold voltage \( V_T \) [19] and the drain voltage for velocity saturation \( V_{DSAT} \), important for carrier and reliability will be affected, although they received as yet far less attention. It has been proposed that the change in \( V_T \) of nMOSFETs with tensile stress \( \sigma \) is given by [20,21]:

\[
q\Delta V_T(\sigma) = (m-1) \left[ \Delta E_g(\sigma) + kT \ln \frac{N_v(0)}{N_v(\sigma)} \right] \quad \text{(uniaxial stress)} \tag{1a}
\]

\[
q\Delta V_T(\sigma) = \Delta E_C(\sigma) + (m-1) \left[ \Delta E_g(\sigma) + kT \ln \frac{N_v(0)}{N_v(\sigma)} \right] \quad \text{(biaxial stress)} \tag{1b}
\]

In Eq. (1), \( m \) is the body-effect coefficient, usually in the range \( 1.3-1.4 \). \( \Delta E_g(\sigma) \) is the band gap reduction with stress and \( \Delta E_C \) is the stress-induced conduction band offset. The latter is negative since due to the stress the energy of the conduction band is lower compared to its value for the unstressed Si. Further, we have that \( q \) is the elementary charge, \( k \) is Boltzmann's constant and \( T \) is the absolute temperature. Finally, \( N_v(0) \) and \( N_v(\sigma) \) are the valence band density of states for the unstrained and strained channel. It is clear that in the first case, the threshold voltage shift results from the change in the band gap and the density of states, while for biaxial stress, also the change in the electron affinity plays a role. Combined with the larger band gap narrowing, this results in a higher \( V_T \) reduction for biaxial compared with CESL-induced tensile stress [19,20]. However, for uniaxial stress associated with Si<sub>x</sub>-Si<sub>x</sub> e-S/D, one has to include the conduction band offset, since in this case, the polysilicon gate is not under stress. Similarly, if the poly-Si gate under the CESL cap is replaced by a metal gate, one has to consider Formulas Eq. (1b) resulting in an expected higher \( V_T \) shift with tensile strain.

Depending on the deformation potential constants, a \( V_T \) shift under tensile strain can be calculated [20], which amounts to \( \sim 10 \text{ mV} \) for a uniaxial and \( -100 \text{ mV} \) for a biaxial strain \( \varepsilon \) of 0.01. At first sight one could for p-channel transistors consider symmetrical formula's to Eq. (1a), i.e., replacing \( N_v \) by \( N_c \) for the n-type substrate and \( \Delta E_C \) by \( \Delta E_V \) if a p<sup>+</sup> polysilicon gate is employed. However, it is important to take into account that for p-channel devices it is necessary to introduce not tensile but compressive stress, implying the need to use SiGe-based structures.

This will result in slightly modified equations. As can be seen from Fig. 2, a \( V_T \) shift of the same order of magnitude \( (100 \text{ mV}) \) can be obtained for c-CESL strained p-channel devices employing a SiON/p<sup>+</sup> polysilicon gate stack. Overall, it can be stated that whatever the sign of the stress, strain engineering usually leads to a reduction of the absolute value of the threshold voltage on the order of 10–100 mV.

![Fig. 2. Threshold voltage in saturation (drain voltage \( V_{DS} = 1 \text{ V} \)) for pMOSFETs with and without c-CESL cap as a function of polysilicon gate length. A 1.5 nm SiON gate dielectric has been employed.](image-url)

2.2. Impact on the gate leakage current

Strain reduces the band gap and at the same time yields a lowering of the conduction band minimum and/or an increase of the valence band maximum in the inversion layer. As a result, the effective barrier height \( \phi_{eff} \) for emission of a carrier across the SiO<sub>2</sub>/Si or Si/high-k interface is expected to increase, so that a reduction of the direct gate tunnelling current across a thin oxide can occur, if the change in the density of states with stress is neglected. The latter will modify the out-of-plane tunnelling effective mass \( m_{eff} \), which alters the tunnelling attempt frequency [22]. In principle, for compressive strain in p- and tensile strain in nMOSFETs, the transverse \( m_{tr} \) will increase, resulting in a lower gate current \( I_G \) [22]. Biaxial and uniaxial tensile strain give the same direction of the conduction band shift and of the out-of-plane mass and should both result in a smaller gate current for electrons. On the other hand, the valence band offset for uniaxial tensile stress is lowered, resulting in a smaller barrier for hole tunnelling and an increase of \( I_G \) [22].

In practice, different trends in the gate current with strain have been observed, whereby other factors, like the bulk oxide and interface traps, the gate voltage or the device length may contribute equally to the resulting change in \( I_G \). In one of the first systematic studies, it was for example reported that the gate current increases for p-channel and reduces for n-channel transistors under external uniaxial tensile stress [22]. The change in gate current density was found in the first instance proportional with the strain \( \varepsilon \), according to:

\[
\Delta I_G/I_G = -t_{ox} \varepsilon \Xi \sqrt{m_{eff} q/2\hbar^2 \phi_{eff}} \tag{3}
\]

with \( t_{ox} \) the gate oxide thickness, \( \hbar \) the reduced Planck constant and \( \Xi \) an effective deformation potential. It was also noted that the strain-induced gate current change was roughly two times less for short compared with long channel transistors [22].

The application of external uniaxial compressive stress enhances the gate current density \( J_G \) for 1.5 nm SiO<sub>2</sub> MOS structures, while little effect was seen for tensile stress [23]. On the other hand, the hole tunnelling current was found to decrease for biaxial and uniaxial compressive stress and to increase for biaxial tensile stress [24]. It was concluded that the strain-induced changes in the valence band offset plays a secondary role compared with the repopulation of the lowest two sub-bands [24]. For Si<sub>x</sub>nMOSFETs in the Fowler–Nordheim (FN) tunnelling regime, the
reduction of $J_G$ has been ascribed to the increase in the FN barrier height [25–28]. On the other hand, at lower gate biases (oxide fields), a higher $J_G$ has been noted and was attributed to a higher oxide-trap-assisted Poole–Frenkel conductance [28]. This already indicates that strain engineering may affect the oxide and interfacial trap density due to the extra processing steps either prior to or after gate stack formation. Finally, it has been observed that the application of longitudinal compressive stress by STI increases the conduction-band electron direct tunnelling current through 1.27-nm gate oxide/n+p poly gate nMOSFETs [29]. It was also proposed to employ the gate current change as a metric to assess the STI-induced strain in the transistors [29].

In the case of local tensile strain by t-CESL or SMT or the combination of both techniques, a significant reduction of $J_G$ can be observed for the n-channel transistors of Fig. 3. The strongest effect is found for the combined CESL and SMT devices. On the contrary, very similar $J_G$ values were obtained for the p-channel transistors processed on the same wafers, using c-CESL caps.

In summary, it is clear that both an increase and a reduction of $J_G$ can be expected depending on the type of stress and carriers considered. Due to the stress, inducing band offsets, there will be a different barrier height for tunnelling through the oxide layer. In addition the stress induced changes of the carrier mass in the inversion layer will modify the tunnel attempt frequency. This means that either an improvement or a degradation of the gate oxide reliability can be anticipated under uniform stress conditions.

2.3. Impact on carrier multiplication

The higher carrier mobility in strained channels implies automatically a lower electric field at velocity saturation and, hence, a lower $V_{DS}$ for the same gate voltage overdrive $V_{GS}$–$V_T$. Consequently, carrier heating in the maximum field $F_{max}$ = $(V_{DS} - V_D)/l$ near the drain becomes easier, resulting in a higher impact ionization current $I_{lq}$ and a higher substrate current $I_{sub}$. This results in a higher multiplication factor $I_{sub}/I_{Dss}$. Hereby is $f$ the characteristic length in the pinch-off region. An additional factor is the strain-induced lowering of the band gap, implying that less energy is lost in the creation of an excess electron–hole pair. This enhanced carrier multiplication should compromise the hot-carrier (HC) reliability of strained devices. This expectation has been confirmed by measurements of the impact ionization and substrate current in strained n- [30–34] and p-channel devices [14,33]. It also explains the lowering of the breakdown voltage of uniaxially strained n-channel SOI MOSFETs [35]. There is only one study, where the effect of strain on the impact ionization of sSi n- and pMOSFETs is found marginal [36], the argument being that in spite of the smaller band gap, the reduced density of states limits the opportunities for scattering. Overall, the consensus is that a higher $I_{lq}$ is observed. Based on that, it has been suggested to exploit this effect in so-called l-MOS devices, in order to reduce the subthreshold slope to values in the sub 5 mV/decade range [37,38].

An additional problem, aggravating the HC problem in sSi devices is the positive temperature coefficient of impact ionization [32]. Combined with the poor thermal conductivity of (Ge) SiGe layers compared with Si [39], self-heating has the potential to increase HC degradation effects in strained MOSFETs under realistic operation conditions. The use of thin virtual substrates in sSi may partially resolve this issue since a reduction of the buffer layer thickness has a positive effect on the thermal resistance [4,40].

3. Impact of strain engineering on the gate oxide and interface quality

It is well-known that the use of a SiGe virtual substrate in sSi may lead to a poorer gate-oxide quality, resulting in a higher density of bulk oxide ($D_{ox}$) or interface traps ($D_{it}$) (for an overview, see e.g. [41]). In turn, this can lead to a higher gate leakage current at low oxide fields [42], owing to for example oxide trap assisted Poole–Frenkel conduction [28]. Different factors can contribute to this higher oxide or interface trap density: the updiffusion of Ge from the virtual substrate to the interface during high thermal budget steps [28,43]; threading dislocations penetrating in the channel region [44–47] and the presence of so-called cross-hatch, related to the misfit dislocations at the bottom interface between the silicon substrate and the SiGe virtual substrate [28]. This leads to enhanced surface roughness [48,49] and a higher density of bulk oxide traps. At the same time, cross-hatch results in strain, and, hence, mobility fluctuations [50].

As LF noise is sensitive to the gate oxide and Si–SiO$_2$ interface traps, it is an appropriate tool to investigate the impact of strain engineering on the quality of the gate dielectric [51].

3.1. sSi n-channel transistors

The impact of global strain engineering, based on sSi on SiGe buffer layers, on the 1/f noise has been extensively studied for n-channel devices [43–48,52–54] (f is the frequency). In most cases, a higher 1/f current noise spectral density $S_f$ has been observed, pointing to a more defective gate oxide compared with unstrained reference devices. The strain has an impact on both the drain and the gate noise spectral density [54]. Different technological parameters contribute to the higher noise. A higher 1/f noise is typically observed for increasing Ge content in the VS [46,53], so that a trade-off exists between higher drive current (mobility), on the one hand, and low 1/f noise operation, on the other. This could be related to the observation that $D_{ox}$ increases with increasing Ge content, as derived from MOS C–V measurements [55]. It has also been observed that reducing the thickness of the VS substrate has a beneficial impact on the 1/f noise [48,53,56,57]. Likewise, using a thicker strained silicon cap has a positive effect on the LF noise [53], which could again be correlated with the lower $D_{ox}$.
and fixed oxide charge, as derived from MOS C–V measurements [55]. Using the drain-current hysteresis technique, it has recently been reported that in sSi devices also a higher number of border traps can be observed compared to unstrained devices [58], thereby increasing the 1/f noise.

However, in some cases, an improvement of the 1/f noise has been observed in sSi nMOSFETs [45,56,59]. As an example, the input-referred noise spectral density ($S_{nC}$) versus gate voltage overdrive is shown in Fig. 4 for 10 $\mu$m $\times$ 1 $\mu$m nMOSFETs processed on standard and sSi substrates. It can clearly be seen that in this case the LF noise is roughly a factor two lower for the sSi devices. As the 1/f noise in the sSi and reference devices behaves according to the unified $\Delta\nu=\Delta\nu_0$ noise theory [60], it can be stated that the lower noise originates from a lower density of traps in the gate oxide. The question arises whether this is a true strain effect or more related to processing aspects?

Clues to an answer on this question can be found in the observation that an in situ thermal tensile stress applied during dry oxidation of (111) Si leads to a reduction of the $P_b$ density, identified by electron spin resonance (ESR) analysis as Si–Si dangling bonds [61]. The opposite is occurring for compressive stress. Therefore, it was postulated that the reduced LF noise is related to an improved oxide quality when an oxide is grown on tensile-strained Si [56]. Recently, this has been confirmed by ESR measurements of the point defects in (100)Si/SiO$_2$ grown at 800°C on biaxially strained Si [62]. As shown in Fig. 5, the trivalent $P_b$-type defects ($P_{b0}$ and $P_{b1}$) decrease with more than 50%. This observation forms the physical basis for the enhanced channel mobility and the lower 1/f noise. In addition, it is beneficial from a reliability viewpoint. For these experiments the dangling bonds are not passivated with hydrogen as for real processed devices. However, even for the latter case a lower density of passivated ($P_{b-H}$) sites reduces the possibility for electrical reactivation during device operation. Also a reduction of the $E^\prime$ centers, related to oxygen vacancies, has been observed. Further work is needed to investigate the impact of strain on the quality of high-$k$ dielectrics.

Of course, one can still argue that noise studies on a well-passivated MOSFET ($D_{ox}$ $\sim$ 10$^{10}$ cm$^{-2}$), where also the oxide traps are partially passivated by hydrogen, is different from ESR studies on a non-passivated oxide, characterized by a $D_{ox}$ of $\sim$ 10$^{12}$ cm$^{-2}$. However, some further support for the positive impact of pre-oxidation tensile strain on the gate oxide quality is provided by the noise studies of Lu et al. [63], demonstrating that for tensile stress induced by STI, a lower 1/f noise is found. They also concluded that the presence of tensile stress before gate oxidation leads to the growth of a better quality oxide with fewer traps. Moreover, recent experimental evidence points to the fact that compressive stress by e-SiGe S/Ds yields a higher density of Si-SiO$_2$ interface traps [64,65], indicating that the presence of strain in the substrate has a clear impact on the formation of dangling bonds.

For good-quality SRB material the dislocation density is in the order of 10$^{11}$ cm$^{-2}$, so that for a small geometry device it is possible to have a “TD-free” transistor [44–47]. However, large-area devices have a higher probability for a TD in the channel, which can give rise to enhanced LF noise [44]. The example shown in Fig. 6 [45] is probably related to a misfit dislocation generated at the strained-Si/SiGe interface, as it is accompanied by a high off-state leakage current. Recently, a channel conductance model has...
been proposed to analyze the effect of a highly localized defect in the channel on the 1/f noise [47].

For completeness, it should be mentioned that a marked reduction of the LF noise was observed for pMOSFETs on sSi substrates with a thick SiGe VS [46].

3.2. Uniaxial tensile strained n-channel transistors

Using a tensile-strained CESL cap enhances the electron mobility. This has been implemented in a 65 nm CMOS technology, with a 1.4 nm decoupled plasma nitride (DPN) gate oxide and a 100 nm polysilicon gate. A typical strain level of 800 MPa can be achieved in this way. As illustrated in Fig. 7 for 1 μm devices the low-frequency 1/f noise is not affected by the t-CESL deposition [66]. For these gate dielectrics, the combination of t-CESL and SMT has no impact on the LF noise [67].

In order to evaluate the effect of the strain on the quality of the gate dielectric, also gate current noise measurements have been performed in devices with different strain techniques: nMOSFETs with tensile strain using SMT, tensile strain using t-CESL, a combination of both (SMT + t-CESL) and references without strain. The devices were fabricated with SiON as a gate dielectric, covered by a polysilicon gate and followed by S/D extension, halo and HDD implants. The different strain techniques were then implemented prior to silicidation. A large sample-to-sample variation was observed in the spectrum of the gate current noise for all devices due to the small transistor area (W × L = 10 μm × 0.13 μm). Therefore, noise data have been averaged over five samples for each type of devices. Fig. 8 shows the measured spectra normalized with respect to the square of the DC gate current for the SMT + t-CESL nMOSFETs and the average normalized spectrum. Note that Lorentzian components are observed in the measured spectra, while the average spectrum shows a clear 1/f dependence. Similar behaviors were observed at different gate voltages and for all types of devices.

Fig. 9 shows the average value of the normalized spectrum evaluated at 10 Hz as a function of the gate voltage. The independence of the normalized gate noise on the gate voltage for all types of devices indicates a uniform energy distribution of oxide traps in the explored energy range. Similar gate current noise levels are observed in components without strain and with different types of strain thus suggesting that the strain can be implemented without increasing the defect density in the gate stack.

While in the previous cases, the use of a tensile cap does not degrade the 1/f noise performance, an improvement of the 1/f noise has been observed when tensile strain was induced either by a local epitaxial SRB layer [44], via STI [63] or by using a t-CESL in fully depleted (FD) SOI nMOSFETs. For the latter, the width and length dependence of the normalized input-referred noise has been studied for 800 MPa tensile CESL strained and standard FD SOI nMOSFETs with 1.5 nm SiON/poly-Si gate stack [68]. The input-referred noise spectral density can be transformed into an oxide trap density [60,68]. The trap density reduces for narrow width CESL devices, while it more or less remains constant for the unstrained counterpart. Only a weak length dependence is observed. To the Authors’ knowledge, so far no results have been reported for Si1−yCy e-S/D pMOSFETs, although, based on what has been found for e-S/D pMOSFETs (see below) little impact is expected.

3.3. Compressively strained p-channel transistors

A detailed performance study of pMOSFETs with either a SiON/poly-Si or HfO2/metal gate stack (1.2–1.4 nm chemical oxide + 1.8–2.0 nm HfO2 + 4 nm TiN + 100 nm poly-Si gate electrode) and with
different strain-engineering approaches (SiGe recessed S/D; 100 nm compressive nitride cap; combination of both) has been carried out. As illustrated in Fig. 10, the strain engineering has only little impact on the LF noise of devices with a SiON/poly-Si gate stack [52]. Also other authors, using different strain engineering approaches, came to the same observation [69].

The experimental observations are, however, quite different for devices with a HfO2 high-k/metal gate stack [16]. In this case strain engineering not only results in a significant increase of the transconductance (23% for cap only, 30% for 15% SiGe and 38% for 25% SiGe S/D plus cap) but has also an impact on the low frequency noise. The noise spectra are typically of the 1/f type with γ close to one.

Fig. 11 points out that the noise increases for devices with a recessed SiGe S/D, independent of the %Ge. The nitride cap has no impact. The quadratic dependence of the normalized drain current noise spectral density on the gate voltage overdrive indicates that the noise is due to number fluctuations [60]. The increase of the noise by a factor of 2 thus corresponds with a doubling of the trap density in the gate stack. The different impact of the two studied

stressors may be due to the fact that during the growth of the epitaxial SiGe recessed layer the thermal budget leads to a recrystallization of the HfO2.

To verify this idea, p-channel transistors with a fully Ni-silicid-ed/HfSiO3/SiO2 gate stack have been investigated. It is anticipated that silicates are more robust and more resistant against the extra thermal budget consisting of an 850 °C pre-epi bake and selective epitaxial deposition at 650 or 750 °C depending on the Ge content (15% or 25%) of the S/D regions. It is shown in Fig. 12 that for these devices there is no marked change in the 1/f noise magnitude, confirming the hypothesis put forward. Also the epi layer thickness has no impact [70].

3.4. Biaxial strained p-channel transistors

The impact of global strain engineering based on strained SiGe layers on silicon substrates has also been studied for both surface and buried channel pMOSFETs. A buried channel can be achieved by depositing a thin silicon cap on top of the SiGe layer, so that the holes flow mainly in the SiGe/Si quantum well, at some distance from the Si/SiO2 interface, resulting in a 1/f lower noise which is dominated by mobility fluctuations [71]. A Si cap layer with a controlled thickness has a positive impact on the noise by reducing the interface roughness. For a too thick Si cap the noise performance equals the behavior of the surface channel devices, while in case of a too thin layer the interface roughness will increase the noise. The carrier confinement in the SiGe channel depends on the Ge concentration and profile. As mentioned before, one also has to take into account the possible impact of the stress on the gate oxide quality and the associated noise performance.

von Haartman et al. [72] systematically studied the noise performance of SiGe pMOSFETs with different Al2O3-based high-k gate dielectrics (Al2O3, Al2O3/HfAlO3/Al2O3 and Al2O3/HfO2/Al2O3) in combination with a TiN gate. In agreement with previous studies, the implementation of a high-k dielectric degrades the noise performance compared to SiO2 mainly due to remote phonon scattering. Of the studied stacks the best results were obtained with HfAlO3. For low gate bias the noise is controlled by the trap density in the dielectric, while for higher bias it becomes scattering dominated [72]. These observations are in agreement with those observed for non strained high-k/metal gate devices.
3.5. Summary LF noise and strain

As illustrated in Section 3.3, the impact of post-oxidation strain-engineering on the 1/f noise is marginal in most cases. The same is observed for p-channel devices with SiON dielectrics. However, in the case of high-κ dielectrics the implementation of post deposition stressors can enhance the 1/f noise, depending on the strain technique used. For p-channels the use of recessed SiGe S/D regions clearly increases the noise, related to the impact of the thermal budget of the epi processing on the recrystallization behavior of the high-κ dielectric, thereby introducing more traps associated with the grain boundaries, while the impact of t-CESL is negligible (see Fig. 11). Further investigations are needed in order to investigate a possible similar impact of tensile SiC or Si1−xCx recessed S/D structures on the 1/f noise of n-channel devices. The used C concentration is typically between 1% and 2%.

An important observation is the fact that there is no unique correlation between the magnitude of the strain and the 1/f noise. This is for both p- and n-channel devices illustrated in Fig. 13, where the strain magnitude is assumed proportional with the change in maximum transconductance (x-axis) and the 1/f noise with the oxide trap density (y-axis). Different tensile (nMOSFETs) and compressive (pMOSFETs) strain techniques are compared. These observations indicate that there is no intrinsic effect of the strain on the 1/f noise, for the process conditions studied here.

It should be remarked that some conflicting data reported in the literature can be due to the influence of some less controlled or unknown process variables. Very often there is no information on whether for measured devices there was Ge outdiffusion or what is the magnitude of the dislocation density. Other process parameters that can have an important influence are the conditions of the gate dielectric formation, additional anneal treatments, etc. LF noise is very sensitive to defects in the dielectric, the interface quality (dangling bond, surface roughness) and substrate defects.

4. Reliability performance of strained devices

Since the mid-eighties, process engineers became aware of the intrinsic strain associated with the gate electrode material and the potential impact on device reliability [73,74]. A more systematic study by applying an external mechanical stress led to opposite conclusions: the change in hot-carrier (HC) degradation was on the one hand, ascribed to a stress-induced change in the formation of interface traps [75], while others concluded that the stress changes the hot carrier generation and not the trapping or HC-induced trap formation [76]. As the devices studied were rather long, the overall effects of stress were rather limited and not of high concern. Nowadays, the applied stress can achieve a decade higher levels, while also much shorter gate lengths are considered, which raises the question about the effect on HC and uniform degrada-
tion. For space and terrestrial applications in a radiation-hash environment, one can equally ask the question about the tolerance of strain-engineered components towards high-doses of ionizing ir-
radiation and particles.

4.1. Hot-carrier degradation of strained nMOSFETs

In order to investigate the impact of strain engineering on gate oxide quality and reliability one has to take into account a variety of parameters such as the type of strain (compressive, tensile, uni-
axial, and biaxial), the applied stress technique (global, recessed S/D, CESL, SMT, etc.), the magnitude of the stress, the channel type (p- or nMOSFETs), the type of gate stack (SiON, HfO2, HfSiOx, poly-Si, FUSI, metal,…) and whether the strain engineering is performed before or after the gate deposition. The fundamental question is whether strain has an intrinsic effect or not.

A substantial amount of data has been gathered in recent years on the HC degradation of sSi nMOSFETs [13,26,31,34,77]. In many cases, a worse HC reliability has been found [13,34], which was mainly ascribed to a higher impact ionization rate. The observations on uniaxial tensile-stressed nMOSFETs are less clear-cut: while some authors find an enhanced HC degradation [12,78,79], others find similar reliability [33,66]. In case of a Si t-CESL cap layer, improvement in the HC reliability has been observed when a 10 nm thick polysilicon buffer layer was inserted between the gate stack and the stressor [79]. For embedded Si1−xCx S/D stressors, again enhanced HC degradation was noted [80,81], ascribed to higher carrier multiplication. Moreover, a strained nFET with [010] orientation was shown to have worse HC resistance over a transistor with a conventional [110] channel, due to increased interface-state generation [81]. At the same time, it was concluded that there were no severe HC reliability constraints for 60nm devices with Si1−xCx S/D stressors.

In the case of t-CESL strained nMOSFETs, fabricated in a 65 nm CMOS technology, negligible effects were found for hot carrier stress at VGS = VDS, as shown in Fig. 14, giving the relative change in the maximum transconductance versus stress time of 0.14 μm long transistors.

![Fig. 13. Trend between the 1/f noise (oxide trap density) and strain magnitude (normalized change in maximum transconductance) for p- and n-channel devices with or without strain engineering.](image)

![Fig. 14. Similar relative gmax degradation (with respect to the unstressed device) induced by hot carrier stress at VGS = VDS is observed in unstressed and t-CESL strained n-MOSFETs. Reported values are averaged over four samples.](image)
4.2. Uniform degradation and BTI of strained MOSFETs

A number of works has studied the time to dielectric breakdown (TTDB) under constant voltage stress of thin oxides grown on sSi substrates [41,82], showing improvement for oxides formed by rapid thermal oxidation using N₂O, followed by N₂ annealing. However, no direct comparison with unstrained reference devices was made.

Therefore, a systematic study of electrical stress-induced degradation of strain-engineered FD SOI devices processed in a 65 nm technology was undertaken. The $V_T$ variation was found to depend on both channel length of the devices and strain level. This is illustrated by the data shown in Fig. 15 for 3 μm and 0.2 μm long transistors [83]. It can be seen that, independent of the gate length and the stress level (SOI, sSOI, and sCESL+SOI), there are two different degradation rates, i.e., an initial degradation by 8–9 mV/decade followed by a degradation with only 20 μV/decade. For all transistor types the change in degradation rate occurs earlier for shorter devices.

The TDDB behavior is illustrated in Fig. 16 for standard (Ref), uniaxial stressed (Unix), biaxial stressed (Biax) and uniaxial + biaxial stressed (Combo) 1 μm × 0.5 μm n-channel SOI devices with 1.5 nm SiON and 100 nm poly-Si gate stack [67]. It can be noticed that there is a reduction from 1.9 V (unstrained) to 1.85 V for biaxially stressed devices and an increase to 2 V for uniaxially strained transistors. This implies that the uniaxial strained devices can operate at high voltages while still satisfying the lifetime requirement of 10 years. It is believed that this improvement is not an intrinsic strain property but rather related to the processing used to implement the strain. For the biaxial strain bonded wafers were used, leading to a poorer oxide quality. In the case of the uniaxial strain the hydrogen content of the CESL layer may have a passivating effect on some of the oxide defects.

A few studies have also been devoted to the Fowler–Nordheim (FN) degradation of strained-Si/SiGe dual-quantum well MOSFETs [84,85]. It was observed that the 1/σ noise of pMOSFETs increases with FN stress. This correlates with the observation of less buried channel operation with increasing stress, i.e., since the current is flowing closer to the Si–SiO₂ interface the impact of carrier scattering becomes more important [84].

For state-of-the-art transistors, NBTI is of great concern and probably one of the most important reliability constraints. It explains the strong interest in the topic in conjunction with strain-engineering [11,13,34,66,86–89]. Aggravated NBTI behavior for pMOSFETs was often found [11,13,86,87] and, in the case of SiN compressive caps ascribed to the excess hydrogen species contained in the strained devices [11]. In order to resolve this issue, a detailed study of SiON/poly-Si devices with SiGe S/D or a combination of SiGe S/D and compressive CESL layers has been undertaken [88], leading to negligible impact on NBTI by the strain engineering, when properly analyzed. Additionally, Arrhenius studies of these devices pointed out that in both unstrained and strained transistors a similar degradation mechanism leads to the observed threshold voltage shifts, lifetime extrapolations and gate length dependence. The similarity in NBTI behavior for devices with and without process-induced strain has also been observed for FUSI/HFSiON devices [89]. These findings are in line with other work, where it was concluded that SiGe S/Ds with an embedded diffusion barrier for controlling B diffusion have improved NBTI behavior compared with strained-Si/SiGe or standard e-SiGe S/D pMOSFETs [34].

Finally, in the case of t-CESL strained nMOSFETs, fabricated in a 65 nm CMOS technology, negligible effects were found in terms of positive bias-temperature instability and TDDB, as shown in Figs. 17 and 18.

Fig. 15. Threshold voltage shift as a function of stress time (constant voltage stress at 2.75 V) in unirradiated FD SOI MOSFETs (W/L = 10 μm/3 μm and W/L = 10 μm/0.2 μm). The degradation depends on the strain level and channel length. Typical behavior is shown for each device type (SOI, sSOI, sCESL + SOI).

Fig. 16. TDDB for reference SOI nMOSFETs and devices with uniaxial, biaxial or combined stress engineering.

Fig. 17. Similar threshold voltage shift induced by bias-temperature stress is observed for unstrained and t-CESL strained nMOSFETs. Reported values are averaged over four samples.
4.3. Degradation under irradiation

As for space applications the use of Commercial-Of-The-Shelf (COTS) devices is becoming common practice, it is of paramount importance to address in an early stage the potential of strain-engineered technologies for such applications. Recently, the radiation hardness of strain engineered SOI devices processed in a 65 nm fully depleted technology has been reported [90]. These devices used a 1.5 nm SiON gate dielectric. The stress in the sSOI wafer was around 1.5–2 GPa, while on other wafers a 100 nm tensile CESL (800 MPa) was implemented. Typical results are shown in Fig. 19 for devices irradiated with $5 \times 10^{11} \text{p/cm}^2$ 60 MeV protons. The selected fluence and energy are typical for the evaluation of electronic circuits to be used for space applications. For nMOSFETs the proton irradiation shifts the front threshold voltage $V_{TF}$ of SOI and sSOI in a positive direction, while it degrades the $V_{TF}$ for the SOI + t-CESL devices. In case of pMOSFETs a $V_{TF}$ decrease is observed for all process conditions. It has to be remarked that independent of the device type, the irradiation results in a build-up of positive charge and interface states in the buried oxide. However, the interaction between the radiation induced charge and the stress impact can be different. A model, based on the passivation/de-passivation of dangling bonds by in-diffusion of hydrogen released from the SiN stressor, has been proposed to explain the experimental observations [90]. It can be stated that for nMOSFETs, the strained Si counteracts the radiation effect of the t-CESL layer. For pMOSFETs, the strained Si reinforces the radiation performance of the t-CESL.

In the case of FinFET devices on SOI substrates, not only the strain but also the device geometry (i.e., fin width, fin height, fin length and number of fins) has an impact on the proton radiation hardness [91]. The effect of a $10^{12} \text{p/cm}^2$ 60 MeV proton irradiation on the electrical performance parameters is illustrated in Table 1 for strained (55 nm Si film with 1.5 GPa biaxial strain on 130 nm buried oxide) and non-strained (65 nm Si film on 145 nm buried oxide) FinFETs with different geometries. The lowest degradation occurs for a single fin structure and increases for wide fins. The hardness reduction is mainly caused by the degradation of the back-channel transistor in relation to the behavior of the backside Si/SiO$_2$ interface.

In addition to the total dose effects, it is also important to investigate the impact of strain on heavy ion irradiation effects. Very recently, first results have been reported on 65 nm strained FD SOI n-channels exposed to 253-MeV I ions [83]. However, it was observed that the irradiation has only a marginal impact on the TDBB, measured subsequently.

Table 1

<table>
<thead>
<tr>
<th></th>
<th>$V_{TF}$ (mV)$^a$</th>
<th>$G_m$ ($\mu$S)$^a$</th>
<th>$\mu_f$ ($\mu$m)$^b$</th>
<th>$R_s$ $^c$</th>
</tr>
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<tbody>
<tr>
<td>Non-strained</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Single fin</td>
<td>&lt;5</td>
<td>$&lt;10^{-2}$</td>
<td>&lt;3</td>
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<tr>
<td>Wide fin</td>
<td>10</td>
<td>20.3</td>
<td>&lt;3</td>
<td>$\uparrow$</td>
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<tr>
<td>Multiple fin</td>
<td>&lt;5</td>
<td>1.05</td>
<td>&lt;3</td>
<td>$\downarrow$</td>
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<tr>
<td>Strained</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Single fin</td>
<td>&lt;5</td>
<td>$&lt;10^{-2}$</td>
<td>10</td>
<td>/</td>
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<tr>
<td>Wide fin</td>
<td>&lt;5</td>
<td>96</td>
<td>&lt;3</td>
<td>$\uparrow$</td>
</tr>
<tr>
<td>Multiple fin</td>
<td>&lt;5</td>
<td>$-19$</td>
<td>&lt;3</td>
<td>$\uparrow$</td>
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</tbody>
</table>

$^a$ Positive numbers correspond to a decrease in $V_{TF}$.

$^b$ Positive numbers correspond to an increase and negative ones to a decrease in the electrical parameter.
Beside the impact of irradiation on the electrical device performance, the question can be asked whether or not irradiation influences the strain in the material. Although the amount of information is very limited, initial experiments indicate that γ-irradiation to a total dose of 51.5 kGy only resulted in a 2.5% relaxation of a Si layer with 0.7–0.8% biaxial tensile strain on a buried oxide (sSiO) [92].

5. Conclusions

It has been shown in most cases, strain engineering, when properly characterized and implemented has only a marginal impact on the oxide quality and does not compromise the long-term reliability aspects. Different observations are found for standard SiON and high-κ gate dielectrics. An important conclusion is that strain has no intrinsic effect on the 1/f noise performance.

Acknowledgments

The authors want to thank R. Agaiby, A. Cester, N. Collaert, G. Eneman, N. Garbar, E. Gerardin, A. Griffoni, M. Jurczak, P. Leroux, R. Loo, N. Lukyanchikova, A. Paccagnella, A. Shickova, A. Steemans, M. Van Uffelen and P. Verheyen for stimulating discussions and the use of some co-authored results. The authors also want to acknowledge the IMEC high-κ, Epi and CMOS-DR teams.

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