Bipolar Mode Operation and Scalability of Double-Gate Capacitorless 1T-DRAM Cells

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Abstract—In this paper, we study the operation mode and the scalability of the second generation (type II) of double-gate capacitorless one transistor dynamic random access memory (1T-DRAM) cells. We find that the memory operates by accumulating charge at the gate interfaces, not in the body of the cell. The type-II configuration allows an infinitely long retention of state “1,” whereas the total retention time is limited by the leakage associated with state “0” due to band-to-band tunneling (BTBT) at the source/drain to bulk junctions. Extensive and careful scaling analysis shows that longitudinal scaling is limited by short-channel effects related to source/drain to bulk barrier lowering, whereas transverse scaling is limited by BTBT. We conclude that type-II 1T-DRAM is somewhat more scalable than type-I 1T-DRAM (i.e., 15 nm versus 25 nm). The better scaling perspective of type-II 1T-DRAM cells is ascribed to the higher READ sensitivity, programming window, and retention time.

Index Terms—Band-to-band tunneling (BTBT), capacitorless 1T-DRAM, device scaling, device simulation, dynamic random access memory (DRAM), impact ionization.

I. INTRODUCTION

S EVERAL years ago, the classical transistor was redesigned to implement a dynamic random access memory (DRAM) cell under the name of zero-capacitor random access memory or, most commonly, 1T-DRAM [1]–[10]. Unlike the classical 1T/1C DRAM cells, the 1T-DRAM memory consisted only of a silicon-on-insulator (SOI) MOSFET but did not require an additional capacitor. The information in 1T-DRAMs is stored in the SOI substrate as excess majority charge created by impact ionization and/or by band-to-band tunneling (BTBT) at the bulk–drain junction induced by the relative high drain voltage. Indeed, the capability of storing charge in the bulk of a MOSFET and the study of its effects on transistor behavior have been discussed since the 1980s [11], [12]. The 1T-DRAM concept is a remarkable example of how an undesirable phenomenon, i.e., the floating-body effect of SOI technology [13], [14], can be transformed into a desirable one, i.e., the storing capacitance of a DRAM cell. Nowadays, 1T-DRAM is drawing a lot of interest from the semiconductor industry storing capacitance of a DRAM cell. Nowadays, 1T-DRAM [13], [14], can be transformed into a desirable one, i.e., the

II. Bipolar Mode Operation of DG 1T-DRAM Cell

As shown in Fig. 1, the 1T-DRAM cell under consideration consists of a DG SOI MOSFET with the two gate contacts connected to the word lines and the source and drain electrodes to the elimination of the additional capacitor; 2) low cost of fabrication, since it is implemented on a standard SOI logic process without exotic process steps; 3) excellent delay–power tradeoff due to the use of SOI technology; and 4) possibility of taking advantage of multigate architectures, as demonstrated in [8]–[10].

Two different types of 1T-DRAM configurations have been proposed. In the first generation of 1T-DRAMs (type I), the electron–hole pairs are created by impact ionization and/or BTBT of inversion charges at the drain end of the transistor. Instead, the stored charge in type-II 1T-DRAM cells consists of the majority carriers injected from the source into the bulk and subsequently collected by the drain field [17]–[20]. The cell works like a bipolar transistor, with the source as the emitter, the bulk as the base, and the drain as the collector. The gate oxide and the SOI substrate prevent the leakage of the excess charge stored in the bulk by applying appropriate potentials at the electrodes. Reports in the literature suggest that type-II 1T-DRAMs have higher READ/WRITE currents, programming window, and retention time compared with the type-I mode [18]. However, the physical mechanism of its operation and the ultimate scalability of the devices have not been studied in detail.

In this paper, we explore the physics of the bipolar operation and the scaling limits of double-gate (DG) type-II 1T-DRAM cells. These cells are sometimes operated in transient mode, with time delay between gate and drain pulses [21]; dc operation of the cells, however, is also possible and provides equivalent capabilities. We will use steady-state cell operation in this scaling study, where the excess charge is accumulated at the gate interfaces and not in the body of the SOI substrate. This reformulation simplifies cell operation and allows explicit comparison of the scaling potential of generation II devices with respect to the scaling limits of type-I cells [22]–[24].

This paper is organized as follows: In Section II, we discuss the physics of the READ/WRITE/HOLD operation for a relative long device length (100 nm). Next, in Section III, we present a scaling analysis about longitudinal and transversal dimensions, i.e., starting from the device structure discussed in Section II, dimensions are reduced, and the implications on READ sensitivity and retention are discussed. Finally, in Section IV, we summarize the conclusions.
connected to the bit lines. The device length (L) and the device width (W) are both 100 nm, the oxide thickness ($t_{ox}$) is 10 nm, and the bulk doping is $10^{17}$ cm$^{-3}$. Two-dimensional device simulations were performed using MEDICI [25] to analyze the operation of the cell, and in addition to the typical drift-diffusion transport model, impact ionization and BTBT models have been explicitly included. At equilibrium, the potentials of all the electrodes are set to zero (in the following, we will refer to this condition as INIT phase). The device is fully depleted due to the short L and W, and the maximum hole concentration in the bulk is around $10^9$ cm$^{-3}$.

**A. WRITE Operations**

As illustrated in Fig. 2, during the WRITE “1” mode (W1), the two gates and the source are held at the same bias, which is negative with respect to the drain bias. The applied bias prevents the creation of inversion charge at the interfaces. Electrons are injected through the source–bulk energy barrier and are collected by the relatively high potential at the drain contact in a manner reminiscent of typical bipolar junction transistors (BJTs). Due to the high longitudinal electric field at the bulk–drain junction, excess electron–hole pairs are created via impact ionization and BTBT processes. Excess electrons are pushed out from the bulk toward the drain due to the favorable field, whereas excess holes are pushed toward the source and are trapped in the bulk if appropriate bias is applied to the electrodes.

Fig. 2 illustrates the bias configuration applied to the structure in the WRITE “0” mode (W0). Source–bulk and drain–bulk energy barriers are lowered by applying negative potentials to the source and drain with respect to the top and bottom gates. This allows removal of the charges previously stored in the WRITE “1” operation.

**B. HOLD Operation**

As illustrated in Fig. 2, during the HOLD mode (H), a negative top/bottom gate to source/drain bias is applied. This bias sets a stationary accumulation condition for the two interfaces. However, if the HOLD operation follows a WRITE “0” operation, then the stationary condition is reached only after a certain delay because the bulk is deeply depleted, and within this delay, the cell remains in state “0.” As will be discussed in detail in Section II-D, the holes necessary to satisfy the accumulation condition are generated by the slow thermal generation processes or BTBT between the source/drain to bulk junctions.

On the other hand, if the HOLD operation follows a WRITE “1” operation, then holes are already present in the bulk because they have been generated by impact ionization and/or BTBT
so that the stationary condition is reached very fast. Most of the excess charge generated during the WRITE “1” phase is lost by leakage through the bulk to source/drain energy barriers, and the rest of the charge is accumulated at the two interfaces so that the self-consistent accumulation condition imposed by the top/bottom gate to source/drain bias is satisfied. This accumulation charge represents the information relative to state “1.”

A number of observations can be made about the operation modes of 1T-DRAM type-II cells. First, the amount of charge representing state “1” does not depend on the actual charge generated during WRITE “1” but only on the negative top/bottom gate to source/drain bias applied during the HOLD mode. The only role of WRITE “1” is speeding up the hole generation rate in the bulk. This means that it is not important to tune exactly the impact ionization/BTBT models in the device simulator nor it is necessary to determine the exact value of the generated excess charge. Of course, the tuning of these models is important for evaluating the WRITE speed. A further advantage of the proposed approach is that, because the value of the accumulated charge is self-consistent with the applied bias, in the HOLD mode, the average hole concentration remains nearly constant for an infinite time. In other words, the retention associated with state “1” is infinity. The retention of the cell information is thus limited by the leakage of state “0,” as will be discussed in Section II-D.

C. READ Operation

As shown in Fig. 2, to implement the READ operation mode (R), the two interfaces are biased asymmetrically and operated in different ways. The top interface works in a way similar to the WRITE “1” mode except that the bulk–drain reverse bias is not large enough to produce excess charge (READ disturb). On the other hand, electrons are injected from the source to the bulk and collected from the drain field, analogous to the bipolar current of a BJT. The bottom interface works as in HOLD mode (i.e., an accumulation condition) since similar potentials are applied at the source and gate electrodes. If the cell is in state “1,” then the accumulation charge at the top interface is lost during READ operation because of the reduced source–bulk barrier. The accumulation charge at the bottom interface, however, is maintained because the bottom interface is in HOLD mode. The excess charge at the bottom interface increases the potential locally, and if the two gates are close to each other, the potential at the top interface is raised as well (gate coupling). The higher potential at the top interface reduces the source–bulk energy barrier, and more electrons are injected, which in turn increases the drain current.

It is interesting to compare the READ currents after WRITE “1” \((I_1)\) and after WRITE “0” \((I_0)\) between the type-I and type-II operation modes (Fig. 3). For this purpose, we evaluated \(I_1\) and \(I_0\) as a function of the top gate voltage with all the other electrodes biased as in the READ mode. At lower (higher) \(V_{TG} - V_S\), the 1T-DRAM cell works in type-II (type-I) mode since the device is biased in the subthreshold (inversion) regime. It is apparent that by moving from type-II toward type-I operation mode, the ratio \(I_1/I_0\) is reduced with the corresponding loss of the programming window. This result reflects the different physical mechanisms governing the impact of the stored holes on the READ current. In the inversion regime of the type-I cells, the stored holes increase the current due to the reduction of threshold voltage through the classical body effect. The READ current in this case is a MOSFET current. Instead, in the subthreshold regime of the type-II cells, the stored holes increase the READ current by lowering the source–bulk energy barrier. The READ current in this case is a bipolar current. Since the current depends exponentially on the bulk potential below threshold (barrier lowering effect) and sublinearly above threshold (body effect), a higher programming window is observed for the type-II operation mode.

D. Transient Analysis

In Fig. 4, we plot as a function of time (a) the average hole concentration in the bulk and (b) the READ drain current for a typical sequence of memory operations. At time \(t = 0\) s, the cell is biased in INIT mode with all the electrode potentials equal to zero. In this condition, the bulk is fully depleted, and the average hole concentration is around \(10^{19}\) cm\(^{-3}\). At time \(t = 10^{-7}\) s, the WRITE “1” bias is applied, and a lot of excess charge is created (around \(10^{19}\) cm\(^{-3}\)). In addition, the drain current is very high due to the large number of excess electrons generated. At time \(t = 10^{-6}\) s, the WRITE “1” bias is removed, and the HOLD bias is applied. The hole concentration reduces very fast, most of the generated charge is lost by source/drain leakage, and the remaining charge is accumulated at the two gate interfaces. Note that in Fig. 4(a) the average hole charge during HOLD mode \((t > 10^{-6}\) s\)) remains constant independent of time because of the self-consistent accumulation condition at the two interfaces. At time \(5 \times 10^{-6}\) s, the READ bias is applied. The average hole concentration reduces roughly by a factor of 2 because of the charge lost at the top interface through the reduced source–bulk energy barrier. The READ drain current is much higher with respect to the READ drain current after INIT because of the stored charge at the bottom interface, which is maintained during the READ operation.
At time $t = 10^{-5}$ s, the WRITE “0” bias is applied. The holes stored at the interfaces rapidly escape through the reduced source–bulk and drain–bulk energy barriers, and the average number of holes in the bulk reduces with respect to the INIT phase. At time $t = 3 \cdot 10^{-5}$ s, the HOLD bias is applied. As already stated, the number of holes increases in the depleted bulk due to thermal generation and BTBT. Finally, at time $t = 10^{-4}$ s, the READ bias is applied. The number of holes increases (READ disturb) because the bottom interface is in the HOLD mode and BTBT occurs. To reduce READ disturbs after a WRITE “0,” 1) the READ pulse should be as short as possible, and 2) the source-bottom gate bias should not be too high to enhance BTBT rates. The READ current in state “0” is very similar to the READ current after INIT, but it is much lower with respect to the READ current after WRITE “1.” This difference in current magnitude allows a high READ sensitivity.

In Fig. 5, the READ currents and the average hole concentration in the bulk after WRITE “0” and WRITE “1” are shown as a function of HOLD time. The reduction of current (hole concentration) after WRITE “1” is due to the source/drain leakage of the residual charge stored in the bulk, whereas the leakage associated with state “0” is due to the hole injection into the bulk caused by BTBT and thermal generation. As already discussed in the previous sections, the retention of the cell is limited by the leakage associated with state “0.” This leakage is due to two different processes occurring during the HOLD mode: the BTBT at the source/drain–bulk junctions and the thermal generation processes in the bulk. In Fig. 6, device simulations have been performed, switching ON and OFF the model for BTBT, and the average hole concentration in the bulk is shown as a function of retention time for two different oxide thicknesses. A stronger leakage associated with state “0” is observed when BTBT is ON, whereas thermal generation is responsible for the leakage in the case of BTBT OFF. Moreover, the impact of BTBT on the leakage in state “0” increases by scaling the transversal geometries ($t_{ox}$ in this case).

### III. Scaling Study of DG 1T-DRAM Cell

With the basic operation of the type-II 1T-DRAM cell established, it is important to explore the scaling potential of such a cell as a function of longitudinal (L) and transverse (W, $t_{ox}$) geometrical parameters. The key performance metrics of this paper are the average hole concentration in the bulk and the READ currents corresponding to the two different states.
The ratio of electrons through the reduced source–bulk barrier at shorter device length is reduced. This is due to the higher injection of electrons from the source increases both currents. The higher bulk potential associated with a lower L and enhanced SCEs reduces the average hole concentration.

A. Longitudinal Scaling (L)

In Fig. 7, we plot as a function of L the average hole concentration and the READ currents corresponding to the two different states after a retention time of 100 ms. As L is reduced, the hole concentration decreases for both states due to the increase in bulk potential induced by enhanced short-channel effects (SCEs). Moreover, since the effect of the bulk potential on the hole concentration is stronger in state “1” due to the higher hole concentration, the difference in hole concentration between the two states decreases with L. It is worth noting that at sufficiently small L, this hole concentration differential disappears since the steady-state condition at the interfaces does not correspond to the accumulation regime, and the 1T-DRAM cell is unable to retain the charge at the interfaces.

The READ currents for both states increase as the device length is reduced. This is due to the higher injection of electrons through the reduced source–bulk barrier at shorter device lengths. The ratio $I_1/I_0$, however, decreases rapidly due to the reduction of the difference in the hole concentration between the two states and due to the reduction in gate coupling, i.e., the influence of the charge at the bottom interface on the potential at the top interface. Indeed, the solution of the 2-D Poisson equation suggests that the increased curvature of longitudinal energy bands associated with the higher SCE produces a lower curvature of energy bands along the transverse direction, so a charge at the bottom interface is less effective in changing the potential at the top interface (low gate coupling). For sufficiently small L, the differential of the hole concentrations vanishes, and the two READ currents coincide. As we will discuss in the next sections, this limiting value for L strongly depends on the transversal geometrical parameters W and $t_{ox}$.

B. Transversal Scaling (W, $t_{ox}$)

In Figs. 8 and 9, we plot the average hole concentration and the READ currents corresponding to the two different states after a retention time of 100 ms as a function of W and $t_{ox}$, respectively. Reducing W ($t_{ox}$) is equivalent to increasing L because it reduces SCE with the corresponding increase in the hole concentration for both states. Both currents reduce because of the lower electron injection from the source into the bulk caused by the higher source–bulk energy barrier. Moreover, in the case of W scaling, the current in state “1” reduces as well because the two gates are closely coupled and the charge stored at the bottom interface is lost during the READ mode due to the low source–bulk energy barrier at the top interface. As W ($t_{ox}$) is reduced, the gate coupling increases, and the ratio $I_1/I_0$ increases as well. When W ($t_{ox}$) is sufficiently low, the steady-state hole concentration in the bulk after WRITE “0” is so high that it is indistinguishable from the accumulation charge stored after WRITE “1,” and as a result, the ratio $I_1/I_0$ starts to decrease. This high hole concentration is ascribed to the BTBT contribution. In fact, as W ($t_{ox}$) is reduced, the longitudinal field at the source/drain to bulk junctions increases, thus enhancing the BTBT. Fig. 6 shows the impact of BTBT on $t_{ox}$ scaling (a similar effect has been observed on W, not shown). Device simulations were performed switching ON and OFF the BTBT model for $t_{ox} = 10$ nm and for $t_{ox} = 7$ nm, and...
the average hole concentration in the bulk is plotted as function of the retention time. It is evident that the hole concentration increase due to the BTBT is stronger at lower of the retention time. It is evident that the hole concentration is not strongly affected. Let us note that \( W_{\text{min}} \) is indeed imposed by a quantum limit to a few nanometers, setting the minimum gate length to \( \sim 15 \) nm.

### C. Summary of Scaling Considerations

We now summarize the scaling properties associated with the DG 1T-DRAM cell working in bipolar operation mode. Let us assume that a higher \( I_1/I_0 \) ratio can be used as a metric of higher READ sensitivity (noise margin), larger programming window, and higher retention time. Transverse scaling of device width and oxide thickness work in a similar manner in reducing SCEs: they both reduce the READ currents but improve their ratio. Nevertheless, transverse scaling is limited by BTBT due to the high hole concentration in state “0,” which can become indistinguishable from the accumulation charge of state “1.” As opposed to transversal scaling, the reduction of L increases the READ currents \( (I_0 + I_1) \) at the expense of a reduced \( I_1/I_0 \). To overcome this problem, \( W \) and/or \( t_{\text{ox}} \) must be scaled as well. The choice of the right geometry \( (L, W, t_{\text{ox}}) \) involves a tradeoff between current amplitudes and READ sensitivity (of the current sense amplifier).

Fig. 10 shows a summary of the scaling of the DG 1T-DRAM cell in bipolar operation mode. Once \( L \) and \( t_{\text{ox}} \) are fixed, a minimum \( W \) (empty symbols) and a maximum \( W \) (filled symbols) \( W \) value are required to have 1) a retention time higher than 100 ms and 2) a ratio \( I_1/I_0 > 10 \) at \( t = 0 \) s (just after WRITE “1”). The retention time is defined as the time necessary for \( I_0 + I_1 \) to reach the average value \( (I_0 + I_1)/2 \) evaluated at \( t = 0 \) s. The presence of a minimum and a maximum for \( W \) is clearly evident from the discussion in Section III-B and Fig. 8. Indeed, as discussed in [22] regarding type-I operation mode, the minimum \( W \) is expected to be imposed by the quantum limit to a few nanometers [26]. It is apparent that, as \( t_{\text{ox}} \) is scaled down, the minimum allowed \( L \) is reduced. We found that for \( t_{\text{ox}} = 8 \) nm, a device length of \( \sim 15 \) nm may be acceptable. It is worth noting that the scaling limit of 15 nm is lower with respect to the 25 nm found for type-I operation mode [22]. However, although the physical reasons of these limits are different, the minimum allowable value of \( W \) that we found is very close to that reported in [22], where quantum models have been turned on. Hence, we expect that the minimum allowable \( L \) that we found is not significantly affected by quantum effects.

As in the case of type-I mode, the source/drain to bulk barrier lowering due to SCEs and the BTBT are the principal factors that limit the device scaling. Nevertheless, the higher READ sensitivity, programming window, and retention time of type-II mode allow better scalability with respect to type-I cells.

### IV. Conclusion

In this paper, we have presented a simulation study aimed at understanding the operation mode, the potential performance in terms of READ sensitivity, programming windows, and retention time, and the scalability of a DG type-II 1T-DRAM cell with respect to type-I cells.

We find that the operations of a type-II 1T-DRAM cell can be implemented by changing simultaneously all electrode potentials and do not necessarily require an appropriate time sequence of bias voltages. Moreover, in the proposed operation mode, the excess charge is stored at the gate interfaces and not in the bulk body. This excess charge is a self-consistent charge, created during the WRITE “1” phase by impact ionization and BTBT at the drain side and defined by the accumulation condition imposed by the gate bias during the HOLD phase. The independence of the stored charge on the particular WRITE “1” bias configuration allows an excellent determination and tuning of device performances by experiments and device simulations.

Stored data are read by an asymmetrical bias configuration of the gate interfaces, where the bottom gate interface works in a manner similar to the HOLD mode, whereas the top gate interface works in a manner similar to the WRITE “1” mode but with a lower drain bias to avoid drain disturbs. The charge eventually stored at the bottom interface increases the bulk potential at the top interfaces, which in turn reduces the source–bulk energy barrier, allowing a high READ current.

Because of the exponential dependence of the READ current with respect to the bulk potential, a higher \( I_1/I_0 \) ratio is found with respect to type-I operation mode (Fig. 3), allowing higher READ sensitivity, programming windows, and retention times.

Data retention is limited by the leakage associated with state “0” due to BTBT at the source/drain to bulk junctions. Except for device geometries with degraded SCEs \( (L \ll W \text{ and/or } t_{\text{ox}}) \), the time retention associated with state “1” is infinity because the stored charge is the self-consistent accumulation charge dictated by gate potentials.

Extensive scaling analysis is done involving longitudinal and transversal geometrical parameters. Longitudinal scaling \( (L) \) is limited by SCEs, which increase the bulk potential and reduce the hole density, hence the retention and the READ sensitivity of state “1.” To compensate this effect, transversal scaling \( (W, t_{\text{ox}}) \) must be used. Moreover, longitudinal scaling increases the absolute value of READ currents. Transversal scaling reduces SCEs, improving the performances of state “1,” but the associated increase of BTBT reduces the performances of state “0.” Moreover, transversal scaling reduces the
absolute value of READ currents. The choice of longitudinal and transverse dimensions is a tradeoff between speed, READ sensitivity, retention, and programming windows. It is found that the scaling limit of device length is around 15 nm, which is lower with respect to the 25 nm found for type-I operation mode [22]. As in the case of type-I mode, the source/drain to bulk barrier lowering due to SCEs and the BTBT are the principal factors that limit the device scaling. Nevertheless, the higher READ sensitivity, programming window, and retention time of type-II mode allow an increased scaling perspective with respect to type-I mode.

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