Physical insights of body effect and charge degradation in floating-body DRAMs

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Abstract

Floating Body one transistor Dynamic Random Access Memories (FBRAMs) have been widely studied and proposed in the literature as an alternative for conventional one transistor/one capacitor DRAMs. FBRAM performance depends on charge degradation during READ and HOLD operations and on the body effect during READ operation, the first setting the amount of the residual non-equilibrium charge during READ operation, and the second setting the effectiveness of this residual charge to modulate the source-body barrier during READ operation. In this work it is proposed a simple analytical charge-based compact model for the body-effect in FBRAMs which is able to reproduce device performance in terms of READ Sense Margin and current ratio. Physical insights of the body effect and charge degradation mechanisms, with particular emphasis to their bias dependence, are discussed in detail. Conclusions can be useful for the choice and the optimization of the bias in FBRAMs. All the discussion is supported by two-dimensional drift–diffusion device simulation on a template double-gate MOSFET.

1. Introduction

Dynamic Random Access Memory (DRAM) technology has rapidly evolved in the last decades, and since the invention of the one-transistor-one-capacitor (1T-1C) cell in the 1960s, chip density has quadrupled every 3 years [1–3]. In the conventional 1T-1C cell the information is stored as charge in the capacitor, so that a direct trade-off between noise margin and scalability exists. Actually 20 nm DRAM technology is in production.

In recent years, at research level, different solutions have been proposed to overcome the scalability issue of 1T-1C cells, one of these being the Floating Body one-transistor DRAMs (FBRAMs) [1–18]. In FBRAMs the cell is composed by a single Silicon On Insulator (SOI) MOSFET and no external capacitor is needed, so that less space is required with respect to conventional 1T-1C DRAMs. Normally, the information is stored as excess charge, with respect to the FRESH condition, in the SOI body generated by non-equilibrium phenomena (band-to-band tunneling and/or impact ionization). The first evidence of a memory effect on SOI substrates has been shown in [7] where a latching behavior was observed due positive feedback between source-body barrier height and excess charge generated by the impact ionization current. However the latching can be hold only if the non-equilibrium generating phenomena in maintained, and this operation mode is not suitable for actual memory operation due to the high power consumption. For this reason, for normal device operation, in the HOLD mode source and drain must be at the same potential and no current flows. Excess charge is generated during the WRITE phase, while it is deleted during the ERASE phase (also called WRITE “1” and WRITE “0” respectively). However, depletion mode can be used as reported in [12]. In this case the equilibrium state is “1” and the current margin is created depleting the body so as to create the require charge imbalance. However, both in the classical and in the depletion operation modes, a charge difference between the reading after WRITE “1” and the reading after WRITE “0” is responsible for the creation of a READ Sense Margin (RSM), defined as the difference between the current read after WRITE (RAW) operation, and the current read after ERASE (RAE) operation. In fact, the higher charge (with respect to RAE) during RAW, reduces the source-body barrier (body-effect), and applying a small drain-to-source voltage, a higher current can be read. In order to consider both classical and depletion operation modes, in the rest of the paper we will refer to the term “excess charge” as the charge difference between RAW and RAE operations.

Depending of the bias condition during READ, the device works in the so called type-I or type-II mode. The higher is the excess charge in the body during RAW operation, the higher is the RSM. However, as we will discuss in Section 4 the maximum excess charge and RSM are limited as function of the bias conditions.

The excess charge is lost over time, due to recombination during HOLD and READ operation, with consequent degradation of the...
RSM. Another possible cause of data degradation is gate leakage. In this paper we will not consider it, assuming that it can be made negligible by a sufficient thick oxide. The degradation process, which sets the ultimate limit of performance of FBRAMs, depends on the device architecture, device size, and bias. The first two factors have been largely discussed in the literature, while less attention has been posed to the influence of the bias on device performance. Because overall device performance can be decoupled in a body-effect contribution and a charge degradation contribution, in this paper the bias dependence on body effect and charge degradation is discussed. In particular, it is proposed a simple analytical charge-based compact model for the body-effect in FBRAMs which is able to reproduce the RSM and the current ratio. Because of the difficulty to measure the excess generated charge, and its relationship with the actual measured current, all the discussion is supported by two-dimensional device simulation on a template double-gate nMOSFET. The rest of the paper is organized as stated in the following. In Section 2 it is presented the architecture of the FBRAM under investigation, its operation, and the physical models used in the device simulator. In Section 3 it is presented the model for the body effect in FBRAMs. In Section 4 it is discussed, on the basis of the proposed model, the dependence of the bias on the body effect and on charge degradation mechanisms in FBRAMs. In particular, in Section 4.1, it is discussed the dependence of the bias during WRITE and READ operations, on the RSM and on charge degradation occurring during READ operation, while, in Section 4.2, it is discussed the dependence of the bias on charge degradation occurring during HOLD operation. Finally, in Section 5, conclusions are summarized.

2. Investigated device structure, modeling and operation

The simulated device structure is a double-gate (DG) MOSFET (Fig. 1a) with gate length \( L = 50 \text{ nm} \), device width \( W = 30 \text{ nm} \), equivalent oxide thickness equal to EOT = 1.1 nm, top and bottom gate workfunction 4.8 eV, source/drain gaussian doping profile with peak value of \( 10^{20} \text{ cm}^{-3} \) at channel edges and standard deviation 2.8 nm. Top and bottom gate are maintained at the same potential \( (V_G) \). The oxide material is SiO\(_2\) and the physical thickness is \( t_{ox} = 1.1 \text{ nm} \). Such small \( t_{ox} \) could produce not negligible data degradation due to gate leakage. However, as stated in the introduction, we are not interested in model gate leakage, and in real applications a higher-\( k \) dielectric material and a higher physical thickness can be used maintaining the same EOT. The body doping is \( 10^{15} \text{ cm}^{-3} \) which, due to the modest device dimensions, results almost undoped.

Two-dimensional MEDICI \([19]\) device simulations (currents are reported in A/\( \mu \text{m} \)) have been performed using the drift–diffusion transport model with Fermi–Dirac statistics and concentration-dependent mobility. Recombination and generation mechanisms include Shockley Read Hall (SRH), Auger, impact ionization, Band-To-Band-Tunneling (BTBT) \([20]\) and Trap-Assisted-Tunneling (TAT) \([20]\). The SRH lifetime is modeled as \( \tau_0[1 + \Gamma(E)] \) where \( \tau_0 \) is a concentration-dependent lifetime modeled as in \([21]\) with parameters as in \([22]\), \( E \) is the electric field, and \( \Gamma(E) > 1 \) is an electric field enhanced factor in order to take into account for TAT. All other model parameters are left to their default value as in the device simulator. WRITE operation is performed through BTBT using a sufficiently large drain-to-gate voltage \([6]\) \( (V_{GS} = -1 \text{ V}) \). This operation mode is normally used to preserve reliability thanks to the low current, but writing operation is slower requiring a sufficiently large pulse width (50 ns in our case). However this choice is not relevant for the discussion in this paper. Generated holes are stored in the body, during HOLD operation, in a potential well created by a sufficiently high source (and drain) to gate voltage \( (V_{GD} = 0) \). The well height sets the longitudinal electric field which is the main responsible for generation and recombination during the HOLD phases due to TAT and BTBT, so that electrode potentials should be chosen in order to obtain the higher retention time. This issue is discussed in Section 4.2. During READ operation (5 ns pulse

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Fig. 1. (a) The simulated device structure is a double-gate (DG) MOSFET with gate length \( L = 50 \text{ nm} \), device width \( W = 30 \text{ nm} \), oxide (SiO\(_2\)) thickness \( t_{ox} = 1.1 \text{ nm} \), gate workfunction 4.8 eV, undoped body, source/drain gaussian doping profile with peak value of \( 10^{20} \text{ cm}^{-3} \) at channel edges and standard deviation 2.8 nm; (b) capacitive model for device operation where \( V_G \) is the gate potential, \( V_{FB} \) is the flat-band voltage, \( V_S \) is the body potential at the top of the source-body barrier, \( C_{ex} \) is the oxide capacitance, \( C_S \) is the body capacitance (inclusive of vertical and horizontal electrostatics), \( Q_{gen} \) is the excess positive charge generated during WRITE, \( C_{gen} \) is the capacitive effect that stores \( Q_{gen} \) and \( T \) is a switch.
width) the presence of excess charge at the body/oxide interfaces affects the body potential and hence the READ current ($V_{DS} = 0.5 \, \text{V}$).

The dependence of the RSM on the READ current is discussed in Sections 4.1 and 4.2. ERASE operation (50 ns pulse width) is performed by applying a sufficient positive gate-to-source/drain voltage ($V_{CS} = 2 \, \text{V}$ and $V_{DS} = 0 \, \text{V}$) in order to reduce the trapping barrier for the stored holes allowing them to flow out. Gate and drain pulses have rising and falling time equal to 1 ns. Bias conditions and timing are summarized in Table 1. In the following, the gate bias actually used during the HOLD and READ phases and drain bias used during WRITE are reported in the related figures.

3. Modeling of body effect and current margin in FBRAMs

In this section it is proposed a charge based compact model from the estimation of the current margin and current ratio in FBRAMs. The modeling is divided in two parts: (i) a charge based model to calculate the potential (hence the body effect) at the top point of the source-body barrier; (ii) classical compact modeling of the drain current in nanoscale saturated MOSFETs [23–26] to calculate the drain current as function of the potential at the top point of the source-body barrier. Such modeling, as all compact models, is affected by a number of approximations, sometimes even strong, with the aim to get out physical insights. The charge based model makes use of a 1D approximation, because the potential at the top of the source-body barrier is calculated using a simplified electrostatic approach along the gate-gate direction, while in compact models for the drain current the only needed information is the value of the potential at the top point of the source-body energy barrier. In such models the assumptions are: (i) 1D carrier transport along the source-drain direction, (ii) drain in saturation, (iii) parabolic band structure at the top point of the source-body energy barrier. All these approximations are included in the proposed model for current margin and current ratio in FBRAMs.

3.1. Charge based model for the body effect in FBRAMs

In order to study the body effect in scaled FBRAMs, let’s consider the very simplified capacitive model for device operation schematized in Fig. 1b where $V_C$ is the gate potential, $V_{DS}$ is the flat-band voltage, $V_S$ is the body potential at the top of the source-body barrier, $C_{OX}$ is the oxide capacitance, $C_S$ is the body capacitance, $Q_{GEN}$ is the excess positive charge generated during WRITE, $T$ is a switch closed only during WRITE operation, and $C_{GEN}$ represents the capacitive coupling effect between the generated charge and the stored charge. The body capacitance $C_S$ is due to the depletion region in the body and includes the effects of both vertical and horizontal electrostatics. Its value is constant in the subthreshold region and $C_S = (m-1) \, C_{OX}$ where $m > 1$ is the subthreshold coefficient.

Let’s consider a sequence ERASE/READ/WRITE/READ. As defined in the introduction, the excess charge is null after ERASE operation although depletion with respect to the FRESH state could be induced [12]. During READ after ERASE (RAE) operation the switch $T$ is open. Because the subsequent READ operation is done in the sub-threshold region $C_S$ can be considered constant, and the body potential is

$$V_{S_{RAE}} = V_{C_{RAE}} \frac{C_{SS}}{C_{SS} + C_{SR}} = \frac{V_{C_{RAE}}}{m}$$

(1)

where $C_{SS}$ is the body capacitance during READ operation. During WRITE operation the switch $T$ is closed, and the change in the body potential due to $Q_{GEN}$ is

$$\Delta V_{S_{SW}} = \frac{Q_{GEN}}{C_{SS} + C_{SW} + C_{GEN}} = \frac{Q_{GEN}}{m_{SW} \, C_{OX}}$$

(2)

where $C_{SW}$ is the body capacitance during WRITE operation. During READ after WRITE (RAW) operation $T$ is open (time $t = 0$) and, at a first order approximation, the body potential can be modeled by an exponential decay

$$V_{S_{RAW}}(t) = [V_{S_{RAW}}(0) - V_{S_{RAW}}(\infty)] e^{-t/T} + V_{S_{RAW}}(\infty)$$

(3)

where $T$ is the decay time constant. Since $V_{S_{RAW}}(\infty) = V_{S_{RAE}}$, the change in body potential (the body-effect), due to the excess charge, between RA and RAW operations is

$$\Delta V_{SR}(t) = V_{S_{RAW}}(t) - V_{S_{RAE}} = \Delta V_{SR}(0) e^{-t/T}$$

(4)

Assuming

$$\Delta V_{SR}(0) = \Delta V_{S_{SW}}; \quad m_{W} \approx m$$

(5)

that is the change of the potential at the top of the source-body barrier, due to $Q_{GEN}$ during WRITE and RAW operation is the same, from Eqs. (2) and (4) the change in body potential becomes

$$\Delta V_{S_{SW}}(t) = \frac{Q_{GEN} \, e^{-t/T}}{m \, C_{OX}}$$

(6)

The term $Q_{GEN} \, e^{-t/T}$ is the excess charge during RAW operation (discussed later) and can be written as $Q_{GEN} \, e^{-t/T} = Q_{RAW}(t) - Q_{RAE} = \Delta Q_{WS}(t)$, where $Q_{RAW}$ and $Q_{RAE}$ are the hole charge during RAW and RAE operation respectively

$$\Delta V_{S_{RAW}}(t) = \frac{\Delta Q_{WS}(t)}{m \, C_{OX}}$$

(7)

The use of the exponential factor $e^{-t/T}$ is rigorous only at the first order, while in the general case it should be substituted with a decay factor $H(t) = \int_0^t Q(t) \, dt$ which is a complex function of SRH lifetime, concentration of the excess charge, availability of electrons for recombination and so on. Based on these considerations, Eq. (7), which could be considered a good approximation also in the case in which a HOLD phase is present between WRITE and READ operations, predicts that the body-effect in FBRAMs increases as the excess charge during RAW increases, and increases, for fixed $C_{OX}$ and $\Delta Q_{WS}$, as device electrostatics improve and short channel effects reduce ($m$ reduces).

3.2. Modeling of the current margin in FBRAMs

In order to model the READ Sense Margin (RSM), let us assume a two-dimensional electron gas at the silicon-oxide interface. Because the drain-to-source voltage during READ (0.5 V) is much higher than the thermal voltage $V_T \sim 25.9 \, \text{mV}$ at room temperature), the READ current is due to source injection only, while drain injection can be considered negligible. Therefore, the RCE current density can be calculated as [23–26]

$$J_{RAW} = A \, T^2 \gamma \, \Sigma_{1/2}(T) = J_0 \, \Sigma_{1/2}(T)$$

(8)

where $A$ is a multiplication constant which takes into account for the band structure, $T$ is the absolute temperature, $\gamma$ is a ballistic coefficient to take into account for the scattering in the channel,
$S_{1/2}$ is the Fermi–Dirac integral of order $1/2$ (in the case of nanowires the order is 0 for one-dimensional electron gas [11] and the order is 1 for three-dimensional electron gas [27]) and $\eta$ is the normalized body potential.

Assuming a heavy doped source region

$$\eta = \frac{E_F - E_{C,max}}{kT} \approx \frac{V_{S,RRAE}}{V_T}$$

where $E_F$ is the source quasi Fermi level, $E_{C,max}$ is the potential energy at the top of the source-body barrier, $k$ is the Boltzmann constant, $V_T = kT/q$ and $q$ is the electronic charge. The RAW current density is therefore

$$J_{RAW} = J_0 S_{1/2}(\eta + \Delta \eta)$$

where

$$\Delta \eta \approx \frac{\Delta V_{SR}}{V_T} \approx \frac{\Delta Q_R}{mV_T C_{ox}}$$

Based on Eqs. (8)–(11), the read sense margin of the current density is

$$J_{RAW} = J_{RAW} - J_{RAE} = J_0 S_{1/2}(\eta + \Delta \eta) - S_{1/2}(\eta) = J_0 S_{0}(\eta, \Delta \eta)$$

while the current density ratio is

$$\frac{J_{RAW}}{J_{RAE}} = \frac{S_{1/2}(\eta + \Delta \eta)}{S_{1/2}(\eta)} = S_{0}(\eta, \Delta \eta)$$

The current-difference factor $S_0(\eta, \Delta \eta)$ and the current-ratio factor $S_0(\eta, \Delta \eta)$ are both decreasing functions of $\eta$ (which increases with the increase of the gate voltage) and increasing functions of $\Delta \eta$ (which increases with the increase of the excess charge). In other words, the current-difference and the current-ratio factors reduce as the READ gate voltage is increased. This dependency explains the higher performances of type-II operation mode [5.8–10] (what is called BJT mode), which operate in the sub-threshold region during RAE operation, over type-I operation mode [4] which operate in weak-strong inversion during both RAE/RAW operations. In particular, for type-II operation, if the excess charge still bias the device in the subthreshold region during RAW, the current-ratio factor $S_0(\eta, \Delta \eta) \approx e^{m \eta}$ (Fermi–Dirac integrals reduce to exponentials in the sub-threshold region) that is it is independent on the gate voltage, and depends only on the excess charge. However, if the excess charge is very high, the device is biased in weak-inversion during RAW and the current-ratio factor depends also on the bias point (gate voltage).

Fig. 2 shows the simulated RAW and RAE currents as function of the READ gate voltage ($V_{G,R}$) in a double-gate nMOSFET with $W = 30$ nm, $L = 50$ nm, $t_{ox} = 1.1$ nm for different values of the drain voltage during WRITE ($V_{D,W}$). Device operation runs through the dynamic sequence ERASE/READ/WRITE/READ (no HOLD operation, $V_{TH,\text{HOLD}} = 0$). The RAW current is checked at the end of the READ pulse (5 ns). Symbols represent the simulated RAW current, while solid lines represent the RAW currents calculated by Eqs. (8)–(11). The values of $m, J_0$ and $V_{SR}$ are extracted by fitting the RAW current (dotted line), while $Q_R$ is calculated by averaging the hole charge in the active device volume at the same time the RAW and RAE currents are checked. Despite the many assumptions of the model, the agreement between the calculated and the simulated RAW currents is very good, especially for the lower values of $V_{D,W}$. Fig. 3 shows that the same concept is valid in devices with different geometry, ranging from $L = 20$ nm to $L = 60$ nm ($W = L/2, t_{ox} = 1.1$ nm). In Fig. 2 the RAW current is just shifted with respect to the RAE current (RAW and RAE current plots are parallel in the sub-threshold region), suggesting that a change in threshold voltage can be defined. Threshold voltage variations are commonly measured as the change in gate voltage necessary to maintain the same current. Based on this definition, equating the expression for the RAW and RAE currents in the sub-threshold region (with different values of $\eta$ corresponding to different gate voltages), the change in threshold voltage, due to the excess charge, is

$$\Delta V_{TH} = -m \Delta V_{SR} = -\frac{\Delta Q_R}{C_{ox}}$$

Eq. (14) can be used for experimental measurement of the residual excess charge $\Delta Q_R$ by the measurement of threshold voltage shift in the subthreshold region ($\Delta V_{TH} \equiv -\Delta V_{SR}$). This result can be for example applied for the experimental measurement of the charge generated by impact ionization and/or band-to-band-tunneling, also in a non-DRAM context. Fig. 4 shows the simulated average excess hole density in the body as a function of the WRITE drain voltage during WRITE operation ($Q_{gen}$), during READ operation ($\Delta Q_R$), and the corresponding $\Delta Q_R$ value calculated by Eq. (14) taking the threshold voltage shift from Fig. 2. The very good agreement between the simulated $\Delta Q_R$ in the subthreshold region ($V_{G,R} = -0.8$ V) and the calculated $\Delta Q_R$ confirms the validity of the proposed body-effect model and assumptions in Eq. (5).

### 4. Body effect and charge degradation in FBRAMs

In this Section it is investigated the dependence of the bias on body-effect and on charge (data) degradation mechanisms. For charge degradation it is intended the decrease (increase) of positive charge after WRITE (ERASE) operation. Charge degradation in FBRAMs occurs during READ and HOLD operations and they will be studied separately in the next subsections. To compare device performances for different bias conditions, the metric cannot be
simply the current ratio neither the current difference. In fact a high current difference can appear with insufficient current ratio and vice versa. Both sufficient current difference and ratio are necessary to sense amplifiers. To this purpose a hybrid metric $H$, can be defined as the product of the current ratio and the current difference

$$H = \frac{I_{RAW}}{I_{RAE}} (J_{RAW} - J_{RAE}) = J_0 \delta_0 (\eta_1, \Delta \eta) \Delta_0 (\eta, \Delta \eta)$$  \hspace{1cm} (15)

The metric $H$ is dominated by the current ratio contribution but has the dimension of a current. In the next two subsections, device performances at different bias conditions will be compared with the metric $H$.

4.1. Body effect and charge degradation during READ

Figs. 4 and 5 show the average hole concentration in the body during WRITE operation, $Q_{gen}$, and the excess $\Delta Q_{gen}$ during RAW operation, as function of $V_{G,R}$ and $V_{D,W}$ for $T_{THOLD} = 0$ (of course $Q_{gen}$ is not function of $V_{G,R}$). As shown in Fig. 4, the higher is $V_{D,W}$ the higher are $Q_{gen}$ and $\Delta Q_{gen}$ so that the RSM and the current-ratio factors increase [Eqs. (12) and (13)]. As stated above, in the subthreshold region the current-ratio $\gamma_R$ is independent on the gate bias point ($\eta$) and depends only on the excess charge $\Delta Q_{gen}$. Fig. 5 shows that the excess $\Delta Q_{gen}$ remains constant as $V_{G,R}$ is increased in the subthreshold region so that $\gamma_R$ remains constant as shown in Fig. 2 (parallel plots in the subthreshold region). As $V_{G,R}$ increases going towards weak and strong inversion, electron concentration is not longer negligible, and recombination of such inversion negative charge with the positive excess charge reduces the excess itself. This reduction, combined with the increase of $\eta$ (due to the higher gate voltage), produces an overall reduction of the RSM and of the current-ratio as shown in Fig. 2. As shown in Fig. 4, the generated excess charge continues to increase in the explored drain bias range and is always higher than the charge retained during READ operation, so that the current saturation observed in Fig. 2 cannot be ascribed to a maximum capacity of the storage capacitance during WRITE operation. The excess charge during READ saturates with respect to $V_{D,W}$ and the saturation WRITE drain voltage depends on $V_{G,R}$. This clearly means that the charge is degraded during READ operation because, above a threshold WRITE drain voltage, the excess charge during READ is independent on the number of holes in the body after WRITE, and depends on the READ bias. This charge saturation, which produces the RAW current saturation observed in Fig. 2, is due to the high excess and related high SRH recombination rate in the first instants of the READ phase. Due to this saturation, for a given $V_{G,R}$, exists a threshold for $V_{D,W}$ above which, the WRITE current and the generated excess charge continue to increases raising the power consumption, but no advantage is obtained in terms of RSM because $\Delta Q_{gen}$ remains constant.

In the rest it is assumed the drain voltage during WRITE equal to this threshold value (1 V in our case) so that the RSM has its maximum with respect to $V_{D,W}$. Assuming RAW current saturation, we can say that, for $T_{THOLD} = 0$, the RSM and the current-ratio $\gamma_R$ increase as $V_{G,R}$ is reduced as shown in Fig. 2 for $V_{D,W} = 1$ V. However a lower limit to $V_{G,R}$ is imposed by the Gate-Induced-Leakage-Current (GIDL), which raises the RAE current with consequent reduction of the current-ratio and RSM.

4.2. Charge degradation during HOLD

Fig. 6 shows the RAW and RAE currents as function of the HOLD time ($T_{THOLD}$) in a DG-nMOSFET with $L = 50$ nm and $W = 30$ nm. Simulations were performed turning on and off the models for TAT and BTBT in the device simulator. The RSM decreases due to SRH generation/recombination and due to BTBT generation at source (drain) to body junction. The SRH contribution is due in turn by band-to-band thermal generation/recombination (source/drain leakage) and by field enhanced generation/recombination due to TAT. As shown in the figure, the main limiting mechanisms for data retention are field enhanced mechanisms that is TAT and BTBT. When TAT and BTBT are turned off the retention time greatly

![Fig. 4](image1)

![Fig. 5](image2)

![Fig. 6](image3)
increases and data retention is limited by SRH band-to-band thermal generation/recombination. TAT helps to restore equilibrium accelerating generation/recombination through a reduced lifetime, while BTBT tends to significantly increment the holes generation during HOLD after ERASE (after WRITE operation the hole generation due to BTBT is less influent because the body is already filled with a lot of holes). Both effects reduce the retention time. Fig. 7 shows the RAW and RAE currents as function of \( T_{\text{HOLD}} \) (TAT and BTBT are turned ON from now on) for different values of the gate voltage during HOLD operation \( V_{\text{CG,H}} \) at fixed READ gate voltage \( V_{\text{GR,R}} = 0.2 \) V. As \( V_{\text{CG,H}} \) is made more negative the READ current at \( T_{\text{HOLD}} \to \infty \), which is the same for both RAW and RAE, increases because the equilibrium hole charge density during HOLD is higher, and the corresponding higher excess charge during READ operation reduces the source-body barrier and increase the READ current. Therefore both RAW and RAE currents, at \( T_{\text{HOLD}} \to \infty \), increase. Reducing the value of \( V_{\text{CG,H}} \) makes the device working from the classical excess charge mode to the depletion mode. In fact, when \( V_{\text{CG,H}} = -0.65 \) V, the equilibrium state is the ERASE state because the hole charge during ERASE is almost equal to the equilibrium hole charge during HOLD and the retention is limited by the recombination of the excess charge generated during WRITE operation. However when \( V_{\text{CG,H}} = -0.85 \) V, the equilibrium state is the WRITE state because the hole charge during WRITE is almost equal to the equilibrium hole charge during HOLD and the retention is limited by the generation of the depleted charge during ERASE operation. For a fixed \( T_{\text{HOLD}} \), the RSM and the current-ratio, as function of \( V_{\text{CG,H}} \), have a maximum, as shown in Fig. 9 in terms of \( H \) (circle symbols) so that this optimum value for \( V_{\text{CG,H}} \) should be chosen. Fig. 8 shows the RAW and RAE currents as function of \( T_{\text{HOLD}} \) for different values of the gate voltage during READ \( V_{\text{GR,R}} \) at fixed HOLD gate voltage \( V_{\text{CG,H}} = -0.75 \) V, the maximum in Fig. 7. For low values of \( T_{\text{HOLD}} \) (≤10 μs) we find the results of the previous section where \( T_{\text{HOLD}} = 0 \), that is the RSM and the current-ratio increase as \( V_{\text{CG,R}} \) is reduced (until the limit imposed by the GIDL current). This is due to the lower electron concentration for lower \( V_{\text{GR}} \) and consequently lower band-to-band thermal recombination during READ, and, especially, due to RAW current saturation. However for \( T_{\text{HOLD}} \to \infty \), strong degradation during HOLD occurs due to TAT/BTBT, and the effect of RAW saturation disappears. For a fixed \( T_{\text{HOLD}} \), the RSM and the current-ratio, as function of \( V_{\text{CG,R}} \), have a maximum, as shown in Fig. 9 in terms of \( H \) (square symbols), so that this optimum value for \( V_{\text{CG,R}} \) should be chosen.

5. Conclusion

In this work the author proposed a simple analytical charge-based compact model for the body-effect in FBRAMs which is able to reproduce the READ Sense Margin (RSM) and the current ratio. Despite the many assumptions of the model, the agreement between the calculated and the simulated RAW currents is very good. Example simulations have been reported for a template double gate MOSFET with undoped body, oxide thickness equal to 1.1 nm, gate length equal to 50 nm, and fin width equal to 30 nm. The method has been demonstrated also to more scaled devices. Physical insights of the body effect and charge degradation mechanisms, with particular emphasis to their bias dependence, have been discussed. Studying the influence of bias during WRITE, HOLD and READ operations it is found that (i) for a given READ gate voltage the RSM saturates at a given WRITE drain voltage (1 V in our case); higher values of WRITE drain voltages will increase the WRITE drain current and the power dissipated during WRITE operation with no advantages in terms of RSM; (ii) the RSM and the current-ratio have a maximum as function of the gate voltage during HOLD \( V_{\text{CH,R}} \), the charge degradation is limited by TAT/BTBT generation/recombination, so that the optimum value of \( V_{\text{CG,R}} \) should be used (0.2 V in our case); (iii) the RSM and the current-ratio have a maximum as function of the gate voltage during READ \( V_{\text{CG,R}} \), the inferior limit imposed by the GIDL current, and the superior limit imposed by thermal band-to-band generation/recombination, so that the optimum value of \( V_{\text{CR}} \) should be used (−0.75 V in our case). Conclusions can be useful for the choice and the optimization of the bias in FBRAMs.
References