Comparative Study of Drain and Gate Low-Frequency Noise in nMOSFETs With Hafnium-Based Gate Dielectrics

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Abstract—In this paper, complementary measurements of the drain and the gate low-frequency noise are used as a powerful probe for sensing the hafnium-related defects in nMOSFETs with high-k gate stacks and polysilicon gate electrode. Drain noise measurements indicate that for low hafnium content (23%) and thin high-k thickness (2 nm), the defect density at the substrate/dielectrics interface is similar to the case of conventional SiO₂. Gate-noise measurements suggest that the defect density in the bulk of the high-k gate stacks and at the gate/dielectrics interface is strongly degraded by the hafnium content.

Index Terms—CMOS reliability, high-k gate dielectric, low-frequency noise.

I. INTRODUCTION

IN ORDER to reduce the gate leakage for the next generation of CMOS devices, the introduction of high-k gate dielectrics is mandatory [1]–[12]. Hafnium-based materials, hafnium oxide (HfO₂) and hafnium silicate oxyxitride (HfSiₓOᵧN_z), are considered the most promising candidates for substituting the conventional SiO₂ or SiON gate dielectrics, because of their high thermodynamic stability on silicon, high permittivity, wide bandgap, and large band offset [1]. Several experimental studies have highlighted that the defect density in Hf-based materials is significantly higher with respect to conventional SiO₂ and SiON gate dielectrics [1]–[12]. These Hf-related defects can act as a trapping center for charge carriers and/or as intermediate states for trap-assisted tunneling or Poole–Frenkel conduction. Consequently, these defects strongly deteriorate the device performance since they cause threshold voltage shift [2], negative and positive bias-temperature instability [3], [6], mobility reduction [4], trap-assisted tunneling [5], and stress-induced leakage current (SILC) [5]. Since the impact of these Hf-related defects diminishes by reducing the high-k stack thickness and/or the Hf content, it is possible to realize a high-quality Hf-based gate stack with ultrathin equivalent oxide thickness (EOT) or with low Hf content. The density of these Hf-related defects has been sensed by using different measurement techniques: capacitance–voltage method [2], threshold voltage shift [2], charge pumping method [5], SILC measurements [5], photocurrent voltage measurements [7], and low-frequency noise measurements [8]–[10]. It is well known that the low-frequency drain-current noise in MOSFET can be used as a powerful probe for sensing the defects close to the substrate/dielectrics interface [13]–[22]. Two fundamental theories have been proposed to explain this low-frequency noise. The first theory is based on the assumption that the channel current noise is due to fluctuations of the number of inversion-layer carriers [16]. These fluctuations are, in turn, due to filling and emptying of charge carriers into trap centers close to the substrate/dielectrics interface. The second theory ascribes the low-frequency channel current noise to the mobility fluctuation [17]. Further, a theory intends to explain the low-frequency noise through a correlated mobility-fluctuation model [18]–[21]. In this model, the trap centers, which generate number fluctuations through trapping and detrapping, act as scattering centers, giving rise to mobility fluctuation. Conversely, only few reports have been dedicated to the study of the gate-current low-frequency noise, which, as it will be shown in this paper, is more sensitive to defects placed in the bulk dielectrics with respect to the drain noise.

The aim of this paper is to investigate the Hf-related defects by means of a comparative study of the low-frequency noise behavior at the drain and at the gate terminal. To this purpose, we have designed and realized a dedicated low-noise measurement system. The remainder of this paper is organized as follows. Section II illustrates the sample device features and the low-noise measurement system. In Section III, we discuss the low-frequency noise measurements at the drain and at the gate terminal. In the conclusions, the main results are summarized.
II. EXPERIMENTAL SETUP

The devices used in this study are nMOSFETs with poly-Si gate, with gate lengths $L$ ranging from 0.18 to 0.25 $\mu$m and with the same gate width $W$ of 10 $\mu$m. Three different gate stacks have been considered: a 2-nm SiO$_2$ layer, a double layer constituted by a 4.5-nm HfO$_2$ film on the top of a 1-nm SiO$_2$ interfacial layer with an EOT of 1.7 nm, and a double layer constituted by a 2-nm Hf$_x$Si$_{1-x}$ON ($x = 0.23$) film on the top of a 1-nm SiON interfacial layer with an EOT of 1.6 nm (see Table I). Hereinafter, for the sake of brevity, we will refer to the three gate stacks as SiO$_2$, HfO$_2$, and HfSiON, respectively.

A detailed dc analysis has been performed by means of the parameter analyzer Keithley 4200-SCS to evaluate gate leakage current, transconductance $g_m$, and threshold voltage $V_T$. HfO$_2$ samples showed a $V_T$ instability at room temperature of about 100 mV, while in all the other samples, the $V_T$ instability was less than 1 mV. The dc analysis was followed by on-wafer noise measurements performed using a purposely designed low-noise measurement system. The core of the system is the low-noise section, which has been enclosed in a metal box placed close to the contacting probes and is battery operated. Two different circuits have been used for the evaluation of the gate-current noise (see Fig. 1) and of the drain-current noise (see Fig. 2). In the case of the gate-current-noise measurement, we have chosen a transimpedance amplifier, due to the high input impedance associated with the gate dielectrics. In the case of the drain-current noise measurement, we resort to a voltage noise amplifier due to the low input impedance associated with the MOSFET channel (a few hundreds ohms). Indeed, the realization of transimpedance amplifiers with an acceptably low noise level and sufficient gain is difficult, due to the problem of the operational amplifier saturation caused by the low device under test (DUT) impedance, which can change significantly with the bias point and with the MOSFET geometry. On the other hand, the gain, and therefore the output voltage, of the voltage amplifier are independent of the DUT impedance. Then, we have evaluated the current drain fluctuations by dividing the drain voltage fluctuations by the channel resistance, since the MOSFETs have been always biased into the linear region. A low-pass filter with a cutoff frequency of 100 mHz has been included in the gate-bias stage (see Fig. 2) to avoid the external interferences coupling with the gate voltage, thus inducing an additional drain noise. In both circuits, each low-noise programmable voltage source has been implemented by means of a 10-$\mu$F polyester capacitor, which can be precharged at the desired voltage level, followed by a low-input-bias-current (1 pA) low-noise operational amplifier (TLC071) connected as a unity-gain buffer. The system allows the synchronous acquisition of the dc and the ac current components and the evaluation of the spectrum of the ac component by means of a PC-based spectrum analyzer.

III. RESULTS AND DISCUSSION

A. Drain Low-Frequency Noise

The drain–current power spectral density $S_{id}$ at different gate bias obtained on nMOSFETs with HfSiON gate dielectrics is reported in Fig. 3. A typical $1/f^\gamma$ behavior with $\gamma$ close to one is observed. The same behavior has been observed also for HfO$_2$ and SiO$_2$ (not shown). The $S_{id}$ normalized with respect to the square of the dc drain current $I_D$ and with respect to the channel length $L$ evaluated at a frequency of 2 Hz as a function of the gate-voltage overdrive is reported in Fig. 4. Two important observations can be made. First, the normalized drain-current noise magnitude is similar for HfSiON and SiO$_2$, thus indicating that at least for low Hf content, the low-frequency-noise performance of nMOSFETs with HfSiON are comparable with the case of conventional gate dielectrics. Second, the
normalized drain-current noise magnitude for HfO\textsubscript{2} is significantly higher with respect to the other investigated gate stacks. In order to estimate the gate-dielectric trap density, we need to understand which mechanism dominates the drain flicker noise. With the MOSFET biased in the linear region, a common method for checking the dominance of number fluctuations is to see if $S_{\text{id}}/I_{\text{D}} \propto (1/N)^2 \propto 1/(V_{\text{GS}} - V_T)^2$, where $N$ is the number of channel electrons [10], [19], [21]. If bulk mobility fluctuations were the main cause of $1/f$ noise, then, from the Hooge formula [17], $S_{\text{id}}/I_{\text{D}} \propto 1/N \propto 1/(V_{\text{GS}} - V_T)$. From Fig. 4, it is clear that in all the three gate stacks, the $1/f$ dominating mechanism is number fluctuations and not bulk mobility fluctuations. The effective volume trap density $N_{\text{ot}}$ is typically extracted by using the formula [18], [20]

$$N_{\text{ot}} = \frac{S_{\text{vg}} \alpha t C_{\text{EOT}}^2 W L f}{q^2 k T I_{\text{D}}^2},$$  

(1)

where $S_{\text{vg}} = S_{\text{id}}/g_m^2$ is the input-referred noise, $q$ is the elementary electron charge, $k T$ is the thermal energy, $\alpha t$ is the tunneling parameter, and $C_{\text{EOT}}$ is the gate-dielectric capacitance per unit area. It is worth noticing that this formula is based on the assumption that $g_m = I_D/(V_{\text{GS}} - V_T)$, i.e., that $g_m$ does not depend on the overdrive gate voltage. Since, in our samples, a strong dependence of $g_m$ on the overdrive gate voltage was observed, we adjust (1) as follows:

$$N_{\text{ot}} = \frac{S_{\text{id}} (V_{\text{GS}} - V_T)^2 \alpha t C_{\text{EOT}}^2 W L f}{q^2 k T I_{\text{D}}^2}.$$  

(2)

As reported in [9], we have used $\alpha t = 10^8$ cm$^{-1}$ for SiO\textsubscript{2}, $\alpha t = 0.5 \times 10^8$ cm$^{-1}$ for HfO\textsubscript{2}, and we have assumed that $\alpha t$ varies linearly with the Hf content $x$ for Hf\textsubscript{x}Si\textsubscript{1-x}ON. By assuming that only traps within $4kT$ of the surface Fermi level contribute to the low-frequency noise, within $z = 2$ nm from the interface (corresponding at $f = 2$ Hz [15]), a rough order of magnitude for the effective surface trap density can be estimated from

$$N_{\text{it}} = 4kT z N_{\text{ot}}.$$  

(3)
Fig. 5. Effective volume trap density $N_{ot}$ and the effective surface trap density $N_{it}$ extracted by the drain flicker-noise measurements as a function of the gate overdrive voltage for different gate materials. The HfO$_2$ gate dielectrics shows higher values of $N_{ot}$ and $N_{it}$ with respect to SiO$_2$ and HfSiON gate dielectrics.

Fig. 6. Power spectral density of the gate current in nMOSFET with HfSiON gate dielectrics at different gate bias.

The obtained results for $N_{ot}$ and $N_{it}$, reported in Fig. 5, indicate that the defect density in the HfO$_2$ layer is more than one decade higher with respect to the other investigated gate stacks.

B. Gate Low-Frequency Noise

The gate-current power spectral density $S_{ig}$ at different gate bias obtained on nMOSFETs with HfSiON gate dielectrics is reported in Fig. 6. A typical $1/f^\gamma$ behavior with $\gamma$ close to one is observed. The same behavior has been observed also for HfO$_2$ and SiO$_2$ (not shown). The $S_{ig}$ normalized with respect to the square of the dc gate current $I_G$ and with respect to the channel length $L$ evaluated at a frequency of 2 Hz as a function of $I_G$ is reported in Fig. 7 for different gate dielectrics. In agreement with the previous results, the higher flicker-noise magnitude is observed for the HfO$_2$ case, whereas in apparent contradiction with the results obtained at the drain terminal, the gate flicker noise of HfSiON is significantly higher with respect to the SiO$_2$ dielectrics. This apparent contradiction can be ascribed to the observation that the drain-current low-frequency noise magnitude depends mainly on the interfacial defects, since these traps cause higher fluctuations of the density and the mobility of the channel charge carriers, whereas the gate-current flicker noise is sensitive to all the defects. As a matter of fact, each charge trapping or detrapping event inside the gate dielectrics alters the local band profile, which influences the tunneling probability coefficient and then the gate current. Thus, the results of Figs. 4 and 7 indicate that although the hafnium introduction in the gate dielectrics always increases the defect density in the entire high-$k$ stack, the interface defectiveness for HfSiON, at least for low Hf content, is similar to the standard SiO$_2$. This observation is in agreement with the results reported in [4] showing similar values of channel electron mobility in nMOSFETs with SiO$_2$ and Hf silicate and a lower value for HfO$_2$.

Furthermore, we have investigated the temperature dependence of the gate flicker noise. As shown in Fig. 8(a), $S_{ig}$ increases with temperature only in the case of HfO$_2$. This effect is due to the strong temperature dependence of the dc gate current $I_G$ observed in HfO$_2$ [5], [23], which indicates that the conduction mechanism is due to trap-assisted tunneling or Poole–Frenkel conduction. Conversely, in SiO$_2$ and HfSiON with low Hf content, the conduction mechanism is mainly due to direct tunneling, thus showing a much weaker temperature dependence [23]. Once we normalize with respect to the square of $I_G$, an almost constant value is obtained also for HfO$_2$ [see Fig. 8(b)], thus indicating that the same noise mechanism is operative in all the explored temperature ranges.

Fig. 7. Normalized gate-current power spectral density evaluated at a frequency of 2 Hz as a function of the dc gate current in nMOSFETs with different gate materials. The hafnium-based high-$k$ gate stacks show a higher low-frequency gate-noise magnitude with respect to conventional SiO$_2$.

Fig. 8. Gate-current power spectral density evaluated (a) at a frequency of 2 Hz and (b) its normalized value, as a function of temperature in nMOSFETs with different gate materials. The normalized values are temperature independent up to 200 °C for all the investigated gate materials.
In this paper, we have experimentally investigated the drain and gate low-frequency noise of nMOSFETs with different high-$k$ gate stacks and similar EOT (ranging from 1.45 to 2 nm) by using a purposely designed low-noise measurement system. It is shown that the gate flicker noise in gate stacks containing hafnium, HfSiON/SiON (2 nm/1 nm), and HfO$_2$/SiO$_2$ (4.5 nm/1 nm) is considerably higher with respect to the reference SiO$_2$. This observation has been ascribed to hafnium-related defects that act as trapping centers for charge carriers, thus causing the gate-current fluctuations. It has been observed that, increasing the temperature up to 200 °C, the noise mechanism does not change for all the investigated gate materials. While also the drain flicker noise in the HfO$_2$/SiO$_2$ (4.5 nm/1 nm) dual-layer stack is considerably higher with respect to SiO$_2$, no significant degradation of the drain flicker noise has been observed for the case of HfSiON/SiON (2 nm/1 nm) with low hafnium content (23%). Since the drain low-frequency-noise magnitude depends mainly on the interfacial defects, our experimental data indicate that for low hafnium content and thin high-$k$ thickness, it is possible to realize high-$k$ gate stacks with an interfacial defect density similar to the case of conventional SiO$_2$.

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REFERENCES


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